





PENTEK

Clock & Sync Generators

CLOCK & SYNC GENERATORS

MODEL	DESCRIPTION
6890	2.2 GHz Clock, Sync and Gate Distribution Board - VME
6891	System Synchronizer and Distribution Board - VME
7190	Multifrequency Clock Synthesizer - PMC
7290, 7390	Multifrequency Clock Synthesizers - 3U/6U cPCI
7690	Multifrequency Clock Synthesizers - PCI
7790	Multifrequency Clock Synthesizers - x16 PCIe
7890	Multifrequency Clock Synthesizer - x8 PCIe
5390	Multifrequency Clock Synthesizer - 3U VPX
7191	Programmable Multifrequency Clock Synthesizer - PMC
7291, 7391	Programmable Multifrequency Clock Synthesizers - 3U/6U cPCI
7691	Programmable Multifrequency Clock Synthesizers - PCI
7791	Programmable Multifrequency Clock Synthesizers - x16 PCIe
7891	Programmable Multifrequency Clock Synthesizer - x8 PCIe
5391	Programmable Multifrequency Clock Synthesizer - 3U VPX
7192	High-Speed Synchronizer and Distribution Board - PMC/XMC
7292, 7392, 7492	High-Speed Synchronizer and Distribution Board - 3U/6U cPCI
7892	High-Speed Synchronizer and Distribution Board - x8 PCIe
5392	High-Speed Synchronizer and Distribution Board - 3U VPX
7893	System Synchronizer and Distribution Board - PCIe
9190	Clock and Sync Generator for I/O Modules
9192	Rack-mount High-Speed System Synchronizer Unit
	Customer Information

Click Here for the PRODUCT SELECTOR

Last updated: January 2013

Model 6890

2.2 GHz Clock, Sync and Gate Distribution Board - VME

ReadyFlow Board Support Package

Features

- Synchronizes up to eight separate boards
- Synchronizes sampling and data acquisition for multichannel systems
- Synchronizes gating and triggering functions
- Clock rates from 800 MHz to 2.2 GHz
- Front panel SMA connectors for clock input and outputs
- Front panel MMCX connectors for gate/trigger and sync signal inputs and outputs
- Single-slot 6U VME board configuration

Ordering Information

Model	Description
6890	2.2 GHz Clock, Sync and Gate Distribution Board - VME

Accessories

Model	Description
2890-00x	Set of Input and Output Cables for two (-002) to eight (-008) boards

General Information

Model 6890 Clock, Sync and Gate Distribution Board synchronizes multiple Pentek I/O boards within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP and software radio applications. Up to eight boards can be synchronized using the 6890, each receiving a common clock of up to 2.2 GHz along with timing signals that can be used for synchronizing, triggering and gating functions.

Input Signals

Model 6890 provides three front panel connectors to accept input signals. One SMA connector is provided for clock signal input, one MMCX connector accepts gate or trigger signals, and another MMCX connector is provided for synchronization. Two additional MMCX connectors are provided for Gate and Sync Enable.

Clock signals are applied from an external source such as a high performance sine wave generator. Gate and sync signals can come from an external source, or from one supported board set to act as the master.

Clock Signals

The 6890 accepts clock input at +10 dBm to +14 dBm with a frequency range from 800 MHz to 2.2 GHz and uses a 1:2 power splitter to distribute the clock. The first output of this power splitter sends the clock signal to a 1:8 splitter for distribution to up to eight boards using SMA connectors.

The second output of the 1:2 power splitter feeds a 1:2 buffer which distributes the clock signal to both the gate and synchronization circuits.

Gate and Synchronization Signals

The 6890 features separate inputs for gate/trigger and sync signals with user-selectable polarity. Each of these inputs can be TTL or LVPECL. Separate Gate Enable and Sync Enable MMCX inputs allow the user to enable or disable these circuits using an external signal.

A programmable delay allows the user to make timing adjustments on the gate and sync signals before they are sent to an LVPECL buffer. A bank of eight MMCX connectors at the output of each buffer delivers signals to up to eight boards.

A 2:1 multiplexer in each circuit allows the gate/trigger and sync signals to be registered with the input clock signal before output, if desired.

Accessories

Model 2890 provides various cable sets with options -002 through -008 supporting synchronization of two to eight boards. Options for individual cables are also available under Model 2890.

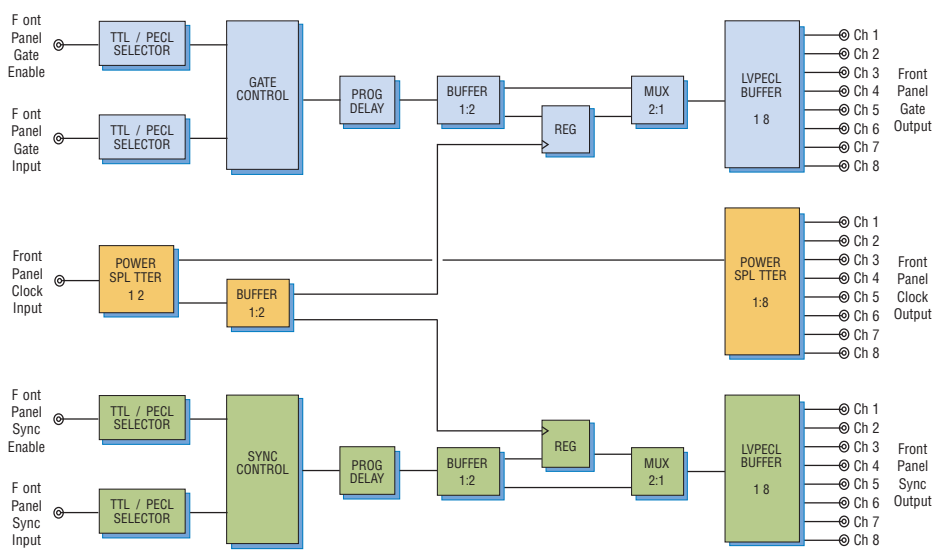
Supported Products

The 6890 currently supports Model 6826 Dual 2 GHz, 10-bit A/D Converter VME Board. Contact the factory for an up-to-date list of supported boards and modules.

Physical Characteristics

Model 6890 is a standard 6U VMEbus board occupying a single VMEbus slot. Dimensions are 160 mm (6.3 inches) deep by 233.5 mm (9.2 inches) high.

The board uses an EMC front panel as specified in IEEE 1101.10. Front panel width is 20.3 mm (0.8 inches).



Model 6891

System Synchronizer and Distribution Board - VME

ReadyFlow Board Support Package

Features

- Synchronizes up to eight separate I/O modules
- Up to eight 6891's can be linked together to synchronize up to 64 I/O modules
- Synchronizes sampling and data acquisition for multichannel systems
- Synchronizes gating and triggering functions
- Clock rates up to 500 MHz
- Front panel SMA connectors for input signals
- Front panel 26-pin Sync Bus connectors compatible with a wide range of Pentek I/O modules
- Single-slot 6U VME board configuration

Ordering Information

Model	Description
6891	System Synchronizer and Distribution Board - VME

Accessories

2891-xxx	Set of Input and Output Cables

General Information

Model 6891 System Synchronizer and Distribution Board synchronizes multiple Pentek I/O modules within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP and software radio applications.

Up to eight modules can be synchronized using the 6891, each receiving a common clock up to 500 MHz along with timing signals that can be used for synchronizing, triggering and gating functions.

For larger systems, up to eight 6891's can be linked together to provide synchronization for up to 64 I/O modules producing systems with up to 256 channels.

Input Signals

Model 6891 provides three front panel SMA connectors to accept TTL input signals from external sources: one for clock, one for gate or trigger and one for a synchronization signal. Two additional SMA connectors are provided for separate gate and sync enable signals.

Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. Alternately, a front panel 26-pin Sync Bus connector accepts LVPECL inputs from any compatible Pentek products to drive the clock, sync and gate/trigger signals.

Output Signals

The 6891 provides eight front panel Sync Bus output connectors, compatible with a wide range of Pentek I/O modules. The Sync Bus is distributed through ribbon cables, simplifying system design.

Clock Signals

The 6891 accepts clock input at +4 dBm to +14 dBm with a frequency range from 1 kHz to 800 MHz. This clock is used to register all sync and gate/trigger signals as well as providing a sample clock to all connected I/O modules.

Gate and Synchronization Signals

The 6891 features separate inputs for gate/trigger and sync signals. Each of these inputs can be TTL or LVPECL. Separate Gate Enable and Sync Enable SMA inputs allow the user to enable or disable these circuits using an external signal.

A programmable delay allows the user to make timing adjustments on the gate and sync signals before they are sent to an LVPECL buffer for output through the Sync Bus connectors.

Cables

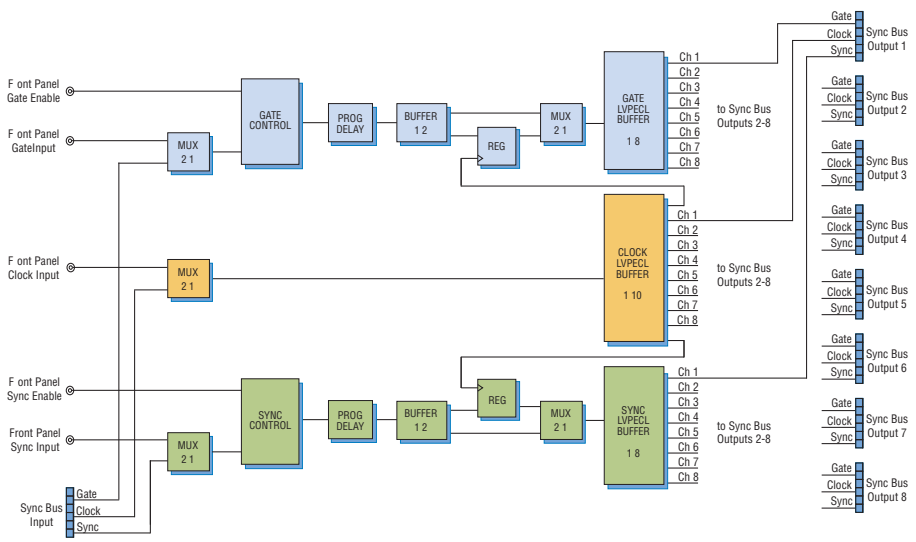
Model 2891 provides various cable kits to support the 6891. Options are available for a range of cable lengths and synchronization of two to eight modules. Options for individual cables are also available under Model 2890.

Supported Products

The 6891 currently supports all models in the 715x family. Contact the factory for an up-to-date list of supported modules.

Physical Characteristics

Model 6890 is a standard 6U VMEbus board occupying a single VMEbus slot.



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New!

Model 7190

Multifrequency Clock Synthesizer - PMC

Features

- Simultaneous synthesis of up to five different clocks
- Eight SMC clock outputs
- Ideal for A/D and D/A converter clock sources
- Typical phase noise: –105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Four quad VCXOs allow selection from 16 different base frequencies
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status via PCI bus interface

ReadyFlow Board Support Package

Ordering Information

Model	Description
7190	Multifrequency Clock Synthesizer - PMC

Options

Specify frequencies of four factory-installed quad VCXOs between 50 and 700 MHz

* Contact Pentek to order specific frequencies

General Information

Model 7190 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board quad VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Clock Synthesizer Circuits

The 7190 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to generate one of four frequencies between 50 and 700 MHz.

The CDC7005 can output the selected frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005's can output up to five frequencies each. The 7190 can be programmed to route any of these 20 frequencies to the module's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs.

With four independent quadVCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7190's can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Interface

The Model 7190 uses an industry-standard 32-bit, 33/66 MHz PCI interface fully compatible with PCI bus specifications. The interface allows reading and writing of status and control signals for setup, operation and monitoring of the module.

Specifications

Front Panel Reference Input
- **Connector Type:** SMC
- **Input Impedance:** 50 ohms
- **Reference Frequency:** 5 to 100 MHz
- **Input Level:** –6 dBm to +10 dBm

PLL Clock Synthesizers & Jitter Cleaners
- **Quantity:** Four
- **Type:** Texas Instruments CDC7005
- **Frequency Dividers:** 1, 2, 4, 8 and 16

Quad VCXOs (Quantity: Four)
- **Frequencies per VCXO:** 4*, software-programmable

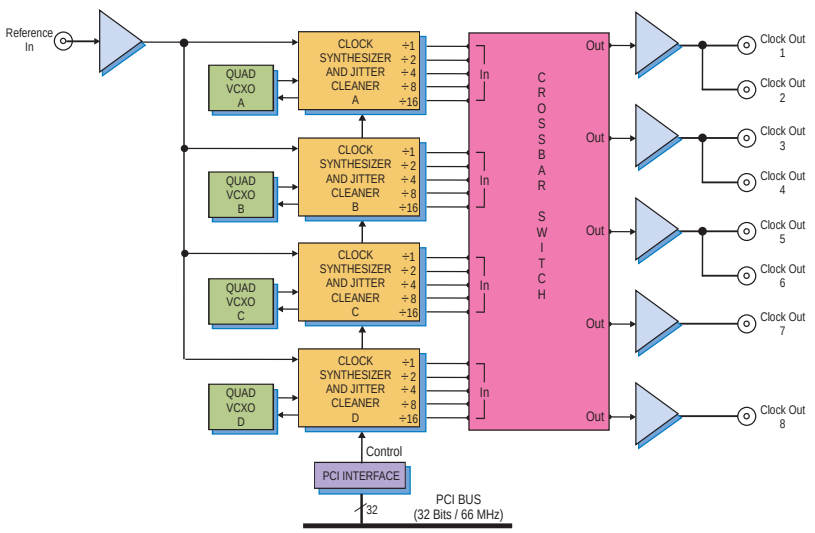
Frequency Range: 50 to 700 MHz
- **Unlocked Accuracy:** ±20 ppm

Front Panel Clock Outputs (Quantity: Eight)
- **Connector Type:** SMC
- **Output Impedance:** 50 ohms
- **Output Level:** +3 dBm @ 700 MHz
- **Typ. Phase Noise:** –105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI Interface
- **PCI Bus:** 32-bit, 66 MHz (supports 33 MHz)
- **Operation:** control and status interface

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard PMC module, 2.91 in. x 5.87 in.



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New!

Models 7290, 7290D and 7390

Multifrequency Clock Synthesizers - 3U/6U cPCI

Model 7390 *Model 7290D*

Features

- Simultaneous synthesis of up to five different clocks
- Eight or 16 SMC clock outputs
- Typical phase noise: –105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Quad VCXOs allow selection from different base frequencies
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status via PCI bus interface

ReadyFlow Board Support Package

Ordering Information

Model	Description
7290	Multifrequency Clock Synthesizer - 6U cPCI
7290D	Dual Multifrequency Clock Synthesizer - 6U cPCI
7390	Multifrequency Clock Synthesizer - 3U cPCI
Options	
	Specify frequencies of four factory-installed quad VCXOs between 50 and 700 MHz

* Contact Pentek to order specific frequencies

General Information

These Models generate up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board quad VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Models 7290 and 7390 generate eight clocks while Model 7290D generates sixteen.

Clock Synthesizer Circuits

These Models use the Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each quad VCXO can be independently programmed to generate one of four frequencies between 50 and 700 MHz.

The CDC7005 can output the selected frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The CDC7005's can output up to five frequencies each. These Models can be programmed to route any of these 20 frequencies to the board's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight or 16 front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all outputs or up to five or ten different clocks to various outputs.

With four or eight independent quad VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where even more different clock outputs are required simultaneously, multiple boards can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Interface

These Models use an industry-standard 32-bit, 33/66 MHz PCI interface fully compatible with PCI bus specifications. The interface allows reading and writing of status and control signals for setup, operation and monitoring of the board.

Specifications

Front Panel Reference Input
- **Connector Type:** SMC
- **Input Impedance:** 50 ohms
- **Reference Frequency:** 5 to 100 MHz
- **Input Level:** –6 dBm to +10 dBm

PLL Clock Synthesizers & Jitter Cleaners
- **Quantity:** Four or eight
- **Type:** Texas Instruments CDC7005
- **Frequency Dividers:** 1, 2, 4, 8 and 16

Quad VCXOs (Quantity: Four or eight)
- **Frequencies per VCXO:** 4*, software-programmable

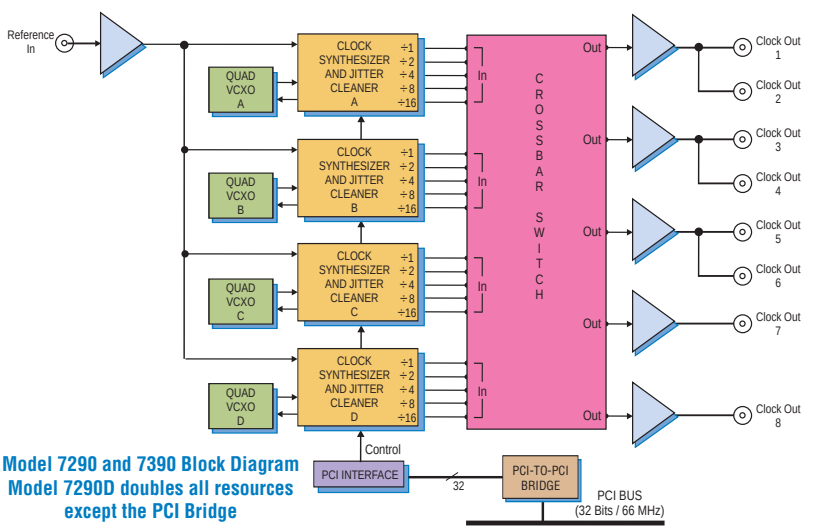
Frequency Range: 50 to 700 MHz
- **Unlocked Accuracy:** ±20 ppm

Front Panel Clock Outputs (Quantity: 8 or 16)
- **Connector Type:** SMC
- **Output Impedance:** 50 ohms
- **Output Level:** +3 dBm @ 700 MHz
- **Typ. Phase Noise:** –105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI Interface
- **PCI Bus:** 32-bit, 66 MHz (supports 33 MHz)
- **Operation:** control and status interface

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard 3U or 6U cPCI board



Model 7290 and 7390 Block Diagram
Model 7290D doubles all resources except the PCI Bridge

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New!

Model 7690

Multifrequency Clock Synthesizer - PCI

Features

- Simultaneous synthesis of up to five different clocks
- Eight SMC clock outputs
- Ideal for A/D and D/A converter clock sources
- Typical phase noise: –105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Four quad VCXOs allow selection from 16 different base frequencies
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status via PCI bus interface

ReadyFlow Board Support Package

Ordering Information

Model	Description
7690	Multifrequency Clock Synthesizer - PCI

Options

Specify frequencies of four factory-installed quad VCXOs between 50 and 700 MHz

* Contact Pentek to order specific frequencies

General Information

Model 7690 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board quad VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Clock Synthesizer Circuits

The 7690 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to generate one of four frequencies between 50 and 700 MHz.

The CDC7005 can output the selected frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005's can output up to five frequencies each. The 7690 can be programmed to route any of these 20 frequencies to the board's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs.

With four independent quadVCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7690's can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Interface

The Model 7690 uses an industry-standard 32-bit, 33/66 MHz PCI interface fully compatible with PCI bus specifications. It attaches directly to computer motherboards with PCI bus slots. Front panel connectors are brought out on the rear panel.

Specifications

Front Panel Reference Input
- **Connector Type:** SMC
- **Input Impedance:** 50 ohms
- **Reference Frequency:** 5 to 100 MHz
- **Input Level:** –6 dBm to +10 dBm

PLL Clock Synthesizers & Jitter Cleaners
- **Quantity:** Four
- **Type:** Texas Instruments CDC7005
- **Frequency Dividers:** 1, 2, 4, 8 and 16

Quad VCXOs (Quantity: 4)
- **Frequencies per VCXO:** 4*, software-programmable

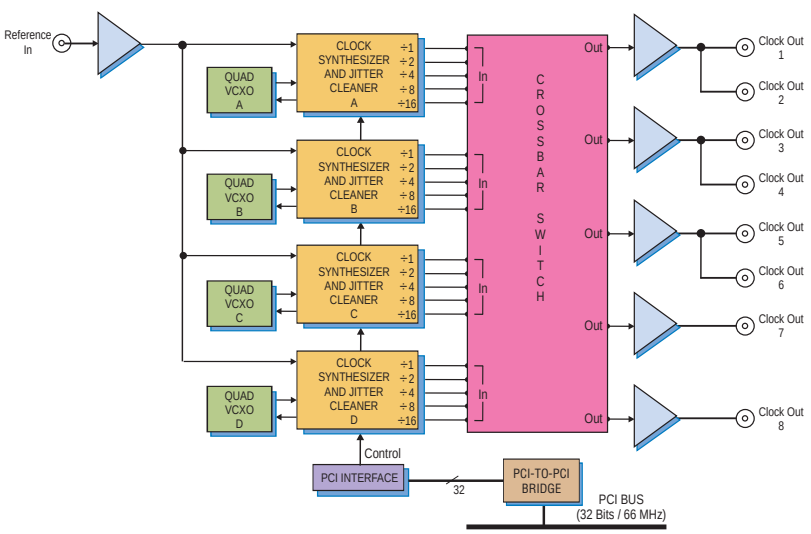
Frequency Range: 50 to 700 MHz
- **Unlocked Accuracy:** ±20 ppm

Front Panel Clock Outputs (Quantity: Eight)
- **Connector Type:** SMC
- **Output Impedance:** 50 ohms
- **Output Level:** +3 dBm @ 700 MHz
- **Typ. Phase Noise:** –105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI Interface
- **PCI Bus:** 32-bit, 66 MHz (supports 33 MHz)
- **Operation:** control and status interface

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard half-length PCI board



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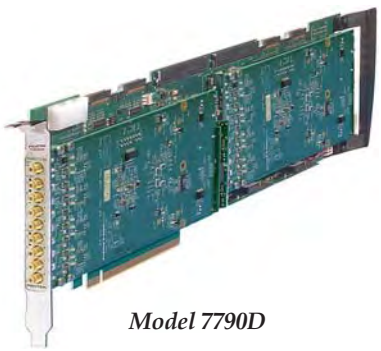
New!

Models 7790, 7790D — Multifrequency Clock Synthesizers - x16 PCIe



Model 7790D

Features

- Simultaneous synthesis of up to five different clocks
- Eight SMC clock outputs
- Ideal for A/D and D/A converter clock sources
- Typical phase noise: –105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Four quad VCXOs allow selection from 16 different base frequencies
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status via PCIe bus interface

ReadyFlow Board Support Package

Ordering Information

Model	Description
7790	Multifrequency Clock Synthesizer - Full-length x16 PCIe
7790D	Dual Multifrequency Clock Synthesizer - Full-length x16 PCIe

Options

Specify frequencies of four factory-installed quad VCXOs between 50 and 700 MHz

* Contact Pentek to order specific frequencies

General Information

These Models generate up to 16 synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters.

These clocks are synthesized from on-board quad VCXOs (voltage controlled oscillators) and can be phase-locked to a reference source.

Model 7790 generates eight clocks while Model 7790D generates sixteen.

Clock Synthesizer Circuits

These Models use the Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each quad VCXO can be independently programmed to generate one of four frequencies between 50 and 700 MHz.

The CDC7005 can output the selected frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The CDC7005's can output up to five frequencies each. These Models can be programmed to route any of these 20 frequencies to the board's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight or 16 front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all outputs or up to five or ten different clocks to various outputs.

With four or eight independent quad VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where even more different clock outputs are required simultaneously, multiple boards can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Express Interface

These Models include a multiple port, 48-lane Gen. 2 PCIe switch with integrated SerDes. The switch provides x16 wide connection to the PCIe interface.

Specifications

Front Panel Reference Input
- **Connector Type:** SMC
- **Input Impedance:** 50 ohms
- **Reference Frequency:** 5 to 100 MHz
- **Input Level:** –6 dBm to +10 dBm

PLL Clock Synthesizers & Jitter Cleaners
- **Quantity:** Four or eight
- **Type:** Texas Instruments CDC7005
- **Frequency Dividers:** 1, 2, 4, 8 and 16

Quad VCXOs (Quantity: Four or eight)
- **Frequencies per VCXO:** 4*, software-programmable

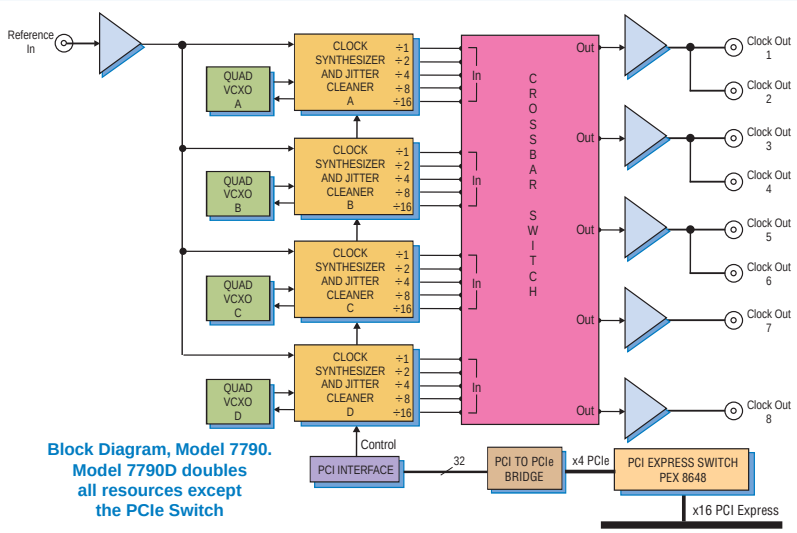
Frequency Range: 50 to 700 MHz
- **Unlocked Accuracy:** ±20 ppm

Front Panel Clock Outputs (Quantity: 8 or 16)
- **Connector Type:** SMC
- **Output Impedance:** 50 ohms
- **Output Level:** +3 dBm @ 700 MHz
- **Typ. Phase Noise:** –105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI to PCIe Interface
- **PCIe Interface:** Gen. 2, x16 width
- **PCIe Ports:** one x4 port to PCI bus, one x16 port to PCIe motherboard
- **Operation:** control and status interface

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Full-length PCIe, 4.38 in. x 12.3 in.



Block Diagram, Model 7790. Model 7790D doubles all resources except the PCIe Switch

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New!

Model 7890

Multifrequency Clock Synthesizer - x8 PCIe

Features

- Simultaneous synthesis of up to five different clocks
- Eight SMC clock outputs
- Ideal for A/D and D/A converter clock sources
- Typical phase noise: –105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Four quad VCXOs allow selection from 16 different base frequencies
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status via PCIe bus interface

ReadyFlow Board Support Package

Ordering Information

Model	Description
7890	Multifrequency Clock Synthesizer - Half-length x8 PCIe

Options

Specify frequencies of four factory-installed quad VCXOs between 50 and 700 MHz

* Contact Pentek to order specific frequencies

General Information

Model 7890 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board quad VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Clock Synthesizer Circuits

The 7890 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to generate one of four frequencies between 50 and 700 MHz.

The CDC7005 can output the selected frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005's can output up to five frequencies each. The 7890 can be programmed to route any of these 20 frequencies to the board's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs.

With four independent quadVCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7890's can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Express Interface

The Model 7890 includes a multiple port, 48-lane Gen. 2 PCIe switch with integrated SerDes. The switch provides x8 wide connection to the PCIe interface.

Specifications

Front Panel Reference Input
- **Connector Type:** SMC
- **Input Impedance:** 50 ohms
- **Reference Frequency:** 5 to 100 MHz
- **Input Level:** –6 dBm to +10 dBm

PLL Clock Synthesizers & Jitter Cleaners
- **Quantity:** Four
- **Type:** Texas Instruments CDC7005
- **Frequency Dividers:** 1, 2, 4, 8 and 16

Quad VCXOs (Quantity: Four)
- **Frequencies per VCXO:** 4*, software-programmable

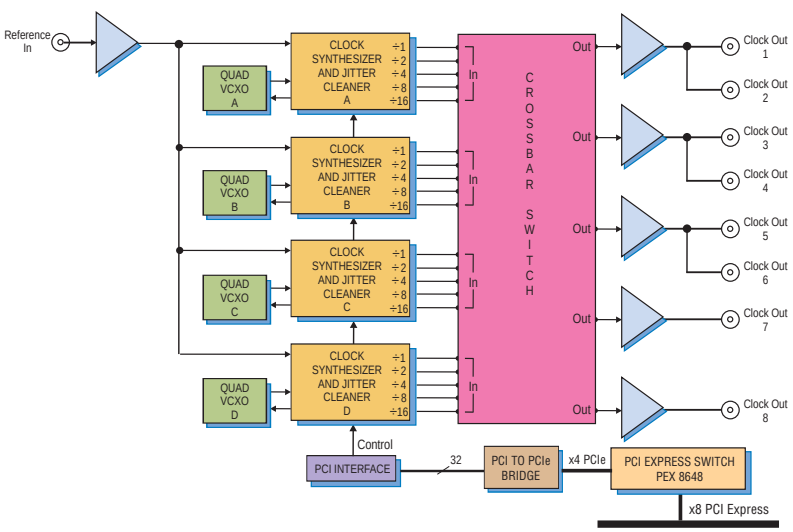
Frequency Range: 50 to 700 MHz
- **Unlocked Accuracy:** ±20 ppm

Front Panel Clock Outputs (Quantity: Eight)
- **Connector Type:** SMC
- **Output Impedance:** 50 ohms
- **Output Level:** +3 dBm @ 700 MHz
- **Typ. Phase Noise:** –105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI to PCIe Interface
- **PCIe Interface:** Gen. 2, x8 width
- **PCIe Ports:** one x4 port to PCI bus, one x8 port to PCIe motherboard
- **Operation:** control and status interface

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Half-length PCIe, 4.38 in. x 6.6 in



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New!

Model 5390

Multifrequency Clock Synthesizer - 3U VPX

Features

- Simultaneous synthesis of up to five different clocks
- Eight SMC clock outputs
- Ideal for A/D and D/A converter clock sources
- Typical phase noise: –105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Four quad VCXOs allow selection from 16 different base frequencies
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status over the VPX backplane

ReadyFlow Board Support Package

Ordering Information

Model	Description
5390	Multifrequency Clock Synthesizer - 3U VPX
Options	
	Specify frequencies of four factory-installed quad VCXOs between 50 and 700 MHz

* Contact Pentek to order specific frequencies

General Information

Model 5390 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board quad VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Clock Synthesizer Circuits

The 5390 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to generate one of four frequencies between 50 and 700 MHz.

The CDC7005 can output the selected frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005's can output up to five frequencies each. The 5390 can be programmed to route any of these 20 frequencies to the board's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs.

With four independent quadVCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 5390's can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Express Switch

Model 5390 includes a PCIe Gen. 2 switch. The switch provides a total of 24 PCIe lanes to the Fabric-Transparent Crossbar Switch on 6 ports. Dynamic lane width negotiation within the PCIe switch allows for x1, x4, x8 or x16 widths.

Specifications

Front Panel Reference Input
- **Connector Type:** SMC
- **Input Impedance:** 50 ohms
- **Reference Frequency:** 5 to 100 MHz
- **Input Level:** –6 dBm to +10 dBm

PLL Clock Synthesizers & Jitter Cleaners
- **Quantity:** Four
- **Type:** Texas Instruments CDC7005
- **Frequency Dividers:** 1, 2, 4, 8 and 16

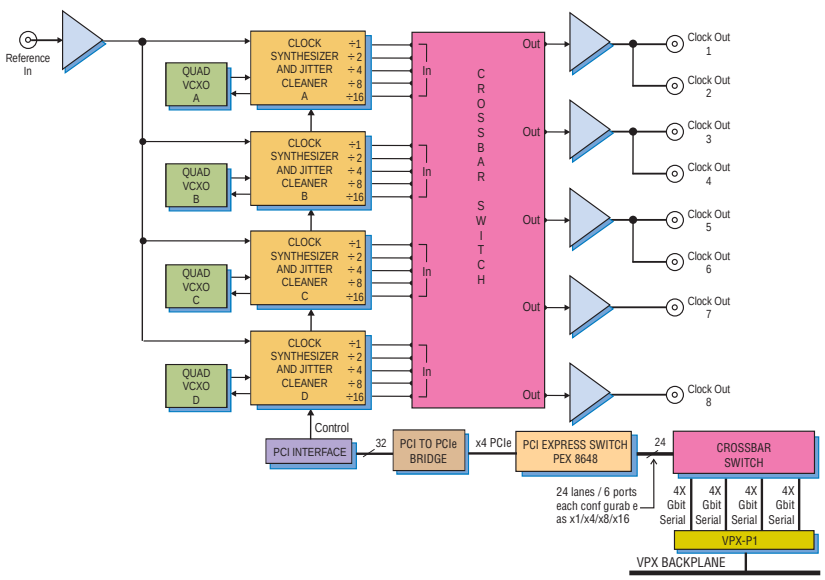
Quad VCXOs (Quantity: Four)
- **Frequencies per VCXO:** 4*, software-programmable

Frequency Range: 50 to 700 MHz
- **Unlocked Accuracy:** ±20 ppm

Front Panel Clock Outputs (Quantity: Eight)
- **Connector Type:** SMC
- **Output Impedance:** 50 ohms
- **Output Level:** +3 dBm @ 700 MHz
- **Typ. Phase Noise:** –105 dBc/Hz @ 1 kHz (dependent on reference source stability)

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)



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New!

Model 7191

Programmable Multifrequency Clock Synthesizer - PMC

Features

- Simultaneous synthesis of up to five different clocks
- Eight SMC clock outputs
- Ideal for A/D and D/A converter clock sources
- Typical phase noise: –105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Four programmable VCXOs with 32-bit tuning resolution
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status via PCI bus interface

ReadyFlow Board Support Package

Ordering Information

Model	Description
7191	Programmable Multifrequency Clock Synthesizer - PMC

General Information

Model 7191 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board programmable VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Clock Synthesizer Circuits

The 7191 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to a desired frequency between 50 and 700 MHz with 32-bit tuning resolution.

The CDC7005 can output the programmed frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005's can output up to five frequencies each. The 7191 can be programmed to route any of these 20 frequencies to the module's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs.

With four independently programmable VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7191's can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Interface

The Model 7191 uses an industry-standard 32-bit, 33/66 MHz PCI interface fully compatible with PCI bus specifications. The interface allows reading and writing of status and control signals for setup, operation and monitoring of the module.

Specifications

Front Panel Reference Input
- **Connector Type:** SMC
- **Input Impedance:** 50 ohms
- **Reference Frequency:** 5 to 100 MHz
- **Input Level:** –6 dBm to +10 dBm

PLL Clock Synthesizers & Jitter Cleaners
- **Quantity:** Four
- **Type:** Texas Instruments CDC7005
- **Frequency Dividers:** 1, 2, 4, 8 and 16

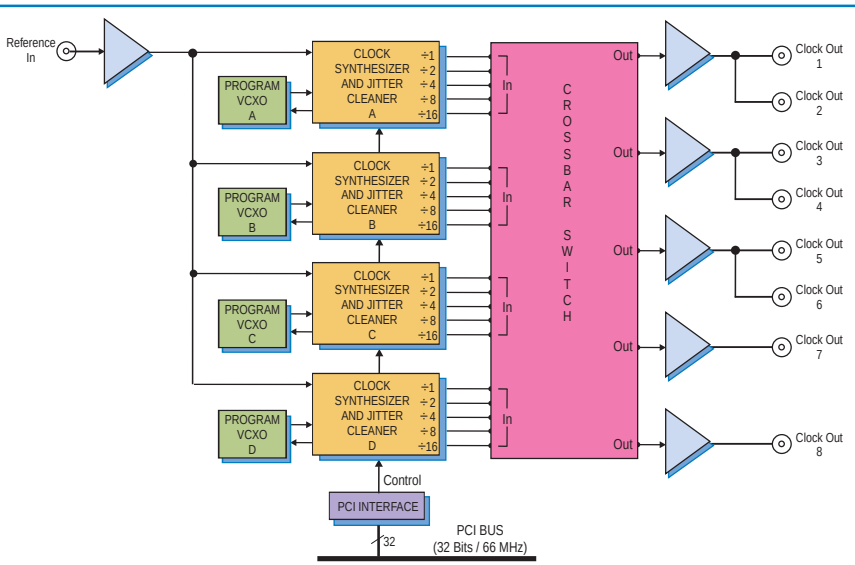
Programmable VCXOs (Quantity: Four)
- **Frequency Range:** 50 to 700 MHz
- **Tuning Resolution:** 32 bits
- **Unlocked Accuracy:** ±20 ppm

Front Panel Clock Outputs (Quantity: Eight)
- **Connector Type:** SMC
- **Output Impedance:** 50 ohms
- **Output Level:** +3 dBm @ 700 MHz
- **Typ. Phase Noise:** –105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI Interface
- **PCI Bus:** 32-bit, 66 MHz (supports 33 MHz)
- **Operation:** control and status interface

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard PMC module, 2.91 in. x 5.87 in.



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New!

Models 7291, 7291D and 7391

Programmable Multifrequency Clock Synthesizers - 3U/6U cPCI

Model 7391 *Model 7291D*

Features

- Simultaneous synthesis of five or ten different clocks
- Eight or 16 SMC clock outputs
- Ideal for A/D and D/A converter clock sources
- Typical phase noise: –105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Four or eight programmable VCXOs with 32-bit tuning resolution
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status via PCI bus interface

ReadyFlow Board Support Package

Ordering Information

Model	Description
7291	Programmable Multifrequency Clock Synthesizer - 6U cPCI
7291D	Dual Programmable Multifrequency Clock Synthesizer - 6U cPCI
7391	Programmable Multifrequency Clock Synthesizer - 3U cPCI

General Information

These Models generate up to 16 synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. Models 7291 and 7391 generate eight clocks while Model 7291D generates sixteen.

Clock Synthesizer Circuits

These Models use fthe Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO (Voltage Controlled Crystal Oscillator) to provide the base frequency for the clock synthesizer. Each of the VCXOs can be independently programmed to a desired frequency between 50 and 700 MHz with 32-bit tuning resolution.

The CDC7005 can output the programmed frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The CDC7005's can output up to five frequencies each. These Models can be programmed to route any of these 20 or 40 frequencies to the board's output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight or 16 front panel SMC connectors supply synthesized clock outputs driven from the five or ten clock output drivers, as shown in the block diagram. This supports a single identical clock to all outputs or up to 16 different clocks to various outputs.

With independently programmable VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than ten different clock outputs are required simultaneously, multiple 7291D's can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Interface

These Models use an industry-standard 32-bit, 33/66 MHz PCI interface fully compatible with PCI bus specifications. The interface allows reading and writing of status and control signals for setup, operation and monitoring of the board.

Specifications

Front Panel Reference Input
- **Connector Type:** SMC
- **Input Impedance:** 50 ohms
- **Reference Frequency:** 5 to 100 MHz
- **Input Level:** –6 dBm to +10 dBm

PLL Clock Synthesizers & Jitter Cleaners
- **Quantity:** Four or eight
- **Type:** Texas Instruments CDC7005
- **Frequency Dividers:** 1, 2, 4, 8 and 16

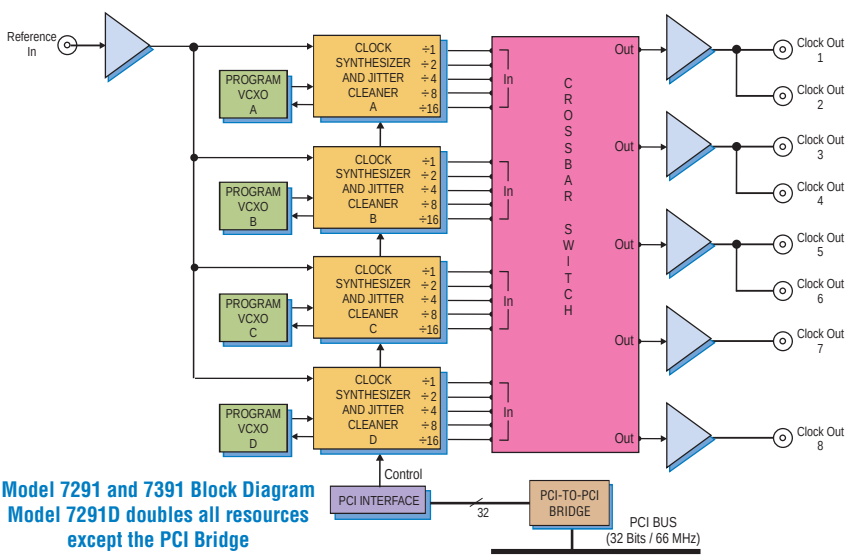
Programmable VCXOs (Quantity: 4 or 8)
- **Frequency Range:** 50 to 700 MHz
- **Tuning Resolution:** 32 bits
- **Unlocked Accuracy:** ±20 ppm

Front Panel Clock Outputs (Quantity: 8 or 16)
- **Connector Type:** SMC
- **Output Impedance:** 50 ohms
- **Output Level:** +3 dBm @ 700 MHz
- **Typ. Phase Noise:** –105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI Interface
- **PCI Bus:** 32-bit, 66 MHz (supports 33 MHz)
- **Operation:** control and status interface

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard 3U or 6U cPCI board.



Model 7291 and 7391 Block Diagram
Model 7291D doubles all resources except the PCI Bridge

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New!

Model 7691

Programmable Multifrequency Clock Synthesizer - PCI

Features

- Simultaneous synthesis of up to five different clocks
- Eight SMC clock outputs
- Ideal for A/D and D/A converter clock sources
- Typical phase noise: –105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Four programmable VCXOs with 32-bit tuning resolution
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status via PCI bus interface

ReadyFlow Board Support Package

Ordering Information

Model	Description
7691	Programmable Multifrequency Clock Synthesizer - PCI

General Information

Model 7691 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board programmable VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Clock Synthesizer Circuits

The 7691 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to a desired frequency between 50 and 700 MHz with 32-bit tuning resolution.

The CDC7005 can output the programmed frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005's can output up to five frequencies each. The 7691 can be programmed to route any of these 20 frequencies to the board's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs.

With four independently programmable VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7691's can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Interface

The Model 7691 uses an industry-standard 32-bit, 33/66 MHz PCI interface fully compatible with PCI bus specifications. The interface allows reading and writing of status and control signals for setup, operation and monitoring of the board.

Specifications

Front Panel Reference Input
- **Connector Type:** SMC
- **Input Impedance:** 50 ohms
- **Reference Frequency:** 5 to 100 MHz
- **Input Level:** –6 dBm to +10 dBm

PLL Clock Synthesizers & Jitter Cleaners
- **Quantity:** Four
- **Type:** Texas Instruments CDC7005
- **Frequency Dividers:** 1, 2, 4, 8 and 16

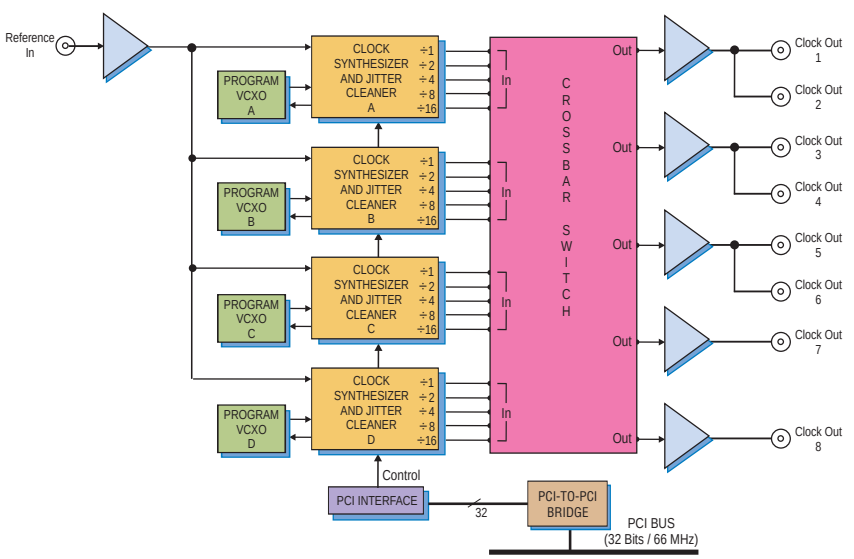
Programmable VCXOs (Quantity: Four)
- **Frequency Range:** 50 to 700 MHz
- **Tuning Resolution:** 32 bits
- **Unlocked Accuracy:** ±20 ppm

Front Panel Clock Outputs (Quantity: Eight)
- **Connector Type:** SMC
- **Output Impedance:** 50 ohms
- **Output Level:** +3 dBm @ 700 MHz
- **Typ. Phase Noise:** –105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI Interface
- **PCI Bus:** 32-bit, 66 MHz (supports 33 MHz)
- **Operation:** control and status interface

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard half-length PCI board



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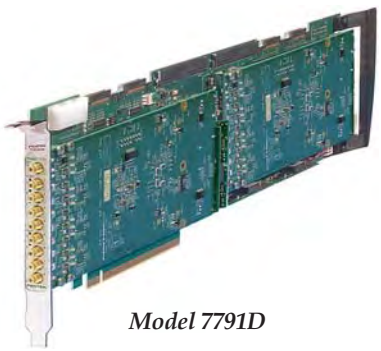
New!

Models 7791, 7791D

Programmable Multifrequency Clock Synthesizers - x16 PCIe



Model 7791D

Features

- Simultaneous synthesis of five or ten different clocks
- Eight or 16 SMC clock outputs
- Ideal for A/D and D/A converter clock sources
- Typical phase noise: –105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Four or eight programmable VCXOs with 32-bit tuning resolution
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status via PCIe bus interface

ReadyFlow Board Support Package

Ordering Information

Model	Description
7791	Programmable Multifrequency Clock Synthesizer - Full-length x16 PCIe
7791D	Dual Programmable Multifrequency Clock Synthesizer - Full-length x16 PCIe

General Information

These Models generate up to 16 synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. Model 7791 generates eight clocks while Model 7791D generates sixteen.

Clock Synthesizer Circuits

These Models use fthe Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO (Voltage Controlled Crystal Oscillator) to provide the base frequency for the clock synthesizer. Each of the VCXOs can be independently programmed to a desired frequency between 50 and 700 MHz with 32-bit tuning resolution.

The CDC7005 can output the programmed frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The CDC7005's can output up to five frequencies each. These Models can be programmed to route any of these 20 or 40 frequencies to the board's output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight or 16 front panel SMC connectors supply synthesized clock outputs driven from the five or ten clock output drivers, as shown in the block diagram. This supports a single identical clock to all outputs or up to 16 different clocks to various outputs.

With independently programmable VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than ten different clock outputs are required simultaneously, multiple 7791D's can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Express Interface

These Models include a multiple port, 48-lane Gen. 2 PCIe switch with integrated SerDes. The switch provides x16 wide connection to the PCIe interface.

Specifications

Front Panel Reference Input
- **Connector Type:** SMC
- **Input Impedance:** 50 ohms
- **Reference Frequency:** 5 to 100 MHz
- **Input Level:** –6 dBm to +10 dBm

PLL Clock Synthesizers & Jitter Cleaners
- **Quantity:** Four or eight
- **Type:** Texas Instruments CDC7005
- **Frequency Dividers:** 1, 2, 4, 8 and 16

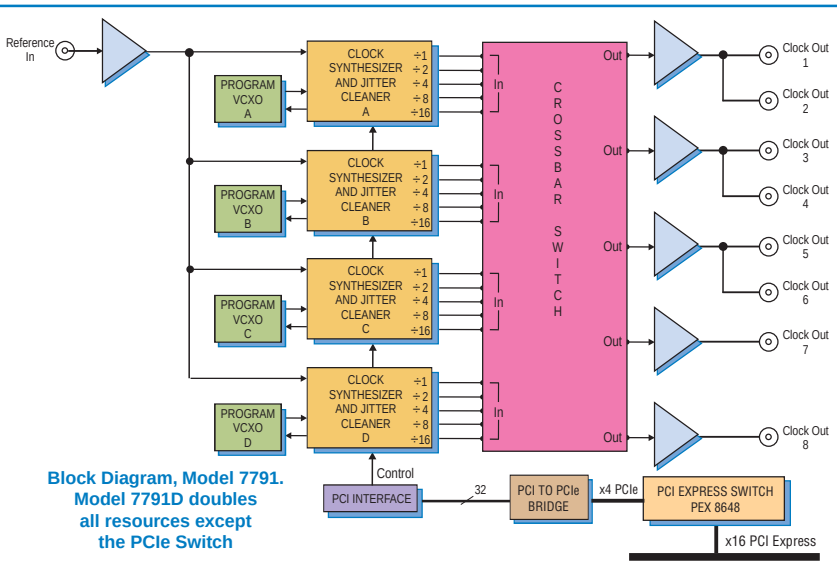
Programmable VCXOs (Quantity: 4 or 8)
- **Frequency Range:** 50 to 700 MHz
- **Tuning Resolution:** 32 bits
- **Unlocked Accuracy:** ±20 ppm

Front Panel Clock Outputs (Quantity: 8 or 16)
- **Connector Type:** SMC
- **Output Impedance:** 50 ohms
- **Output Level:** +3 dBm @ 700 MHz
- **Typ. Phase Noise:** –105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI to PCIe Interface
- **PCIe Interface:** Gen. 2, x16 width
- **PCIe Ports:** one x4 port to PCI bus, one x16 port to PCIe motherboard
- **Operation:** control and status interface

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Full-length PCIe, 4.38 in. x 12.3 in.



Block Diagram, Model 7791. Model 7791D doubles all resources except the PCIe Switch

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New!

Model 7891

Programmable Mulrifrequency Clock Synthesizer - x8 PCIe

Features

- Simultaneous synthesis of up to five different clocks
- Eight SMC clock outputs
- Ideal for A/D and D/A converter clock sources
- Typical phase noise: –105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to 100 MHz
- Four programmable VCXOs with 32-bit tuning resolution
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status via PCIe bus interface

ReadyFlow Board Support Package

Ordering Information

Model	Description
7891	Programmable Multifrequency Clock Synthesizer - Half-length x8 PCIe

General Information

Model 7891 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board programmable VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Clock Synthesizer Circuits

The 7891 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to a desired frequency between 50 and 700 MHz with 32-bit tuning resolution.

The CDC7005 can output the programmed frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005's can output up to five frequencies each. The 7891 can be programmed to route any of these 20 frequencies to the board's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs.

With four independently programmable VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7891's can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Express Interface

The Model 7891 includes a multiple port, 48-lane Gen. 2 PCIe switch with integrated SerDes. The switch provides x8 wide connection to the PCIe interface.

Specifications

Front Panel Reference Input
- **Connector Type:** SMC
- **Input Impedance:** 50 ohms
- **Reference Frequency:** 5 to 100 MHz
- **Input Level:** –6 dBm to +10 dBm

PLL Clock Synthesizers & Jitter Cleaners
- **Quantity:** Four
- **Type:** Texas Instruments CDC7005
- **Frequency Dividers:** 1, 2, 4, 8 and 16

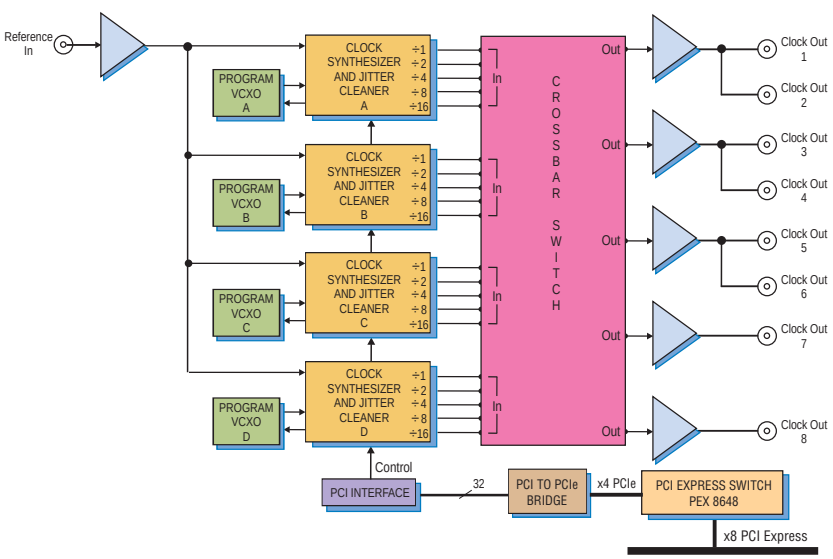
Programmable VCXOs (Quantity: Four)
- **Frequency Range:** 50 to 700 MHz
- **Tuning Resolution:** 32 bits
- **Unlocked Accuracy:** ±20 ppm

Front Panel Clock Outputs (Quantity: Eight)
- **Connector Type:** SMC
- **Output Impedance:** 50 ohms
- **Output Level:** +3 dBm @ 700 MHz
- **Typ. Phase Noise:** –105 dBc/Hz @ 1 kHz (dependent on reference source stability)

PCI to PCIe Interface
- **PCIe Interface:** Gen. 2, x8 width
- **PCIe Ports:** one x4 port to PCI bus, one x8 port to PCIe motherboard
- **Operation:** control and status interface

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Half-length PCIe, 4.38 in. x 6.6 in.



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New!

Model 5391

Programmable Multifrequency Clock Synthesizer - 3U VPX

Features

- Simultaneous synthesis of up to five different clocks
- Eight SMC clock outputs
- Ideal for A/D and D/A converter clock sources
- Typical phase noise: –105 dBc/Hz @ 1 kHz offset
- All clocks are phase-locked to input reference signal
- Input reference frequency of 5 to100 MHz
- Four progammable VCXOs with 32-bit tuning resolution
- Output clocks of 1, 2, 4, 8, or 16 submultiples of VCXO base frequencies
- Output clock frequencies between 50 and 700 MHz
- Control and status over the VPX backplane

ReadyFlow Board Support Package

Ordering Information

Model	Description
5391	Programmable Multifrequency Clock Synthesizer - 3U VPX

General Information

Model 5391 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board programmable VCXOs (voltage controlled oscillators) and can be phase-locked to an external reference signal.

Clock Synthesizer Circuits

The 5391 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to a desired frequency between 50 and 700 MHz with 32-bit tuning resolution.

The CDC7005 can output the programmed frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005's can output up to five frequencies each. The 5391 can be programmed to route any of these 20 frequencies to the board's five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference clock. This reference is a 5 to 100 MHz signal supplied to a front panel SMC connector.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers, as shown in the block diagram. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs.

With four independently programmable VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 5391's can be used and phase-locked with a 5 to 100 MHz system reference.

PCI Express Interface

Model 5390 includes a PCIe Gen. 2 switch. The switch provides a total of 24 PCIe lanes to the Fabric-Transparent Crossbar Switch on 6 ports. Dynamic lane width negotiation within the PCIe switch allows for x1, x4, x8 or x16 widths. These can be selected in any combination.

Specifications

Front Panel Reference Input
- **Connector Type:** SMC
- **Input Impedance:** 50 ohms
- **Reference Frequency:** 5 to 100 MHz
- **Input Level:** –6 dBm to +10 dBm

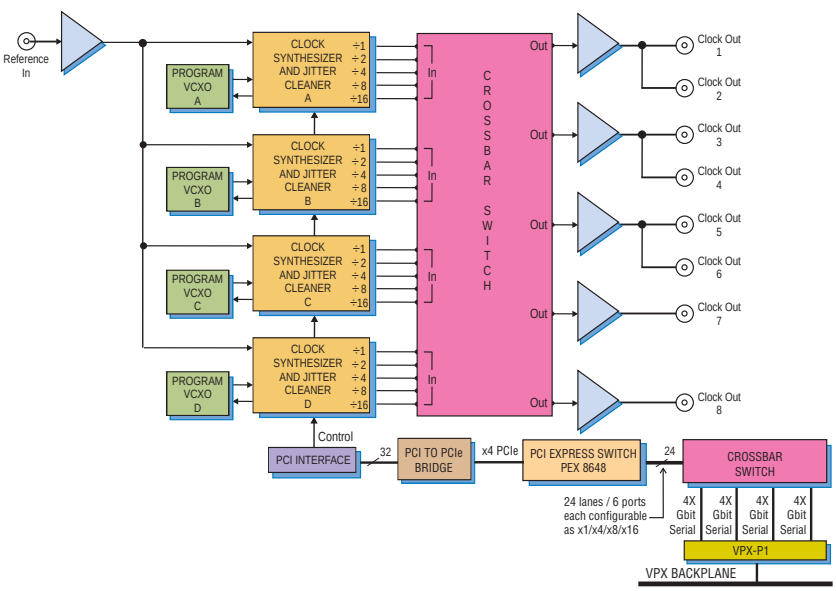
PLL Clock Synthesizers & Jitter Cleaners
- **Quantity:** Four
- **Type:** Texas Instruments CDC7005
- **Frequency Dividers:** 1, 2, 4, 8 and 16

Programmable VCXOs (Quantity: Four)
- **Frequency Range:** 50 to 700 MHz
- **Tuning Resolution:** 32 bits
- **Unlocked Accuracy:** ±20 ppm

Front Panel Clock Outputs (Quantity: Eight)
- **Connector Type:** SMC
- **Output Impedance:** 50 ohms
- **Output Level:** +3 dBm @ 700 MHz
- **Typ. Phase Noise:** –105 dBc/Hz @ 1 kHz (dependent on reference source stability)

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)



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New!

Model 7192

High-Speed Synchronizer and Distribution Board - PMC/XMC

ReadyFlow Board Support Package

Features

- Synchronizes up to four separate high-speed Cobalt or Onyx I/O modules
- Synchronizes sampling and data acquisition for multichannel systems
- Synchronizes gating and triggering functions
- Clock rates up to 1.8 GHz
- Front panel MMCX connectors for input signals
- Front panel µSync connectors compatible with a range of Pentek Cobalt and Onyx modules

General Information

The Model 7192 High-Speed Synchronizer and Distribution Board synchronizes multiple Pentek Cobalt or Onyx modules within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP, and software radio applications.

Up to four modules can be synchronized using the 7192, with each receiving a common clock along with timing signals that can be used for synchronizing, triggering and gating functions.

Input Signals

Model 7192 provides three front panel MMCX connectors to accept input signals from external sources: one for clock, one for gate or trigger and one for a synchronization signal. Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. In addition to the MMCX connector, a reference clock can be accepted through the first front panel µSync output connector, allowing a single Cobalt or Onyx board to generate the clock for all subsequent boards in the system.

Output Signals

The 7192 provides four front panel µSync output connectors, compatible with a range of high-speed Pentek Cobalt and Onyx modules. The µSync signals include a reference clock, gate/trigger and sync signals and are distributed through matched cables, simplifying system design.

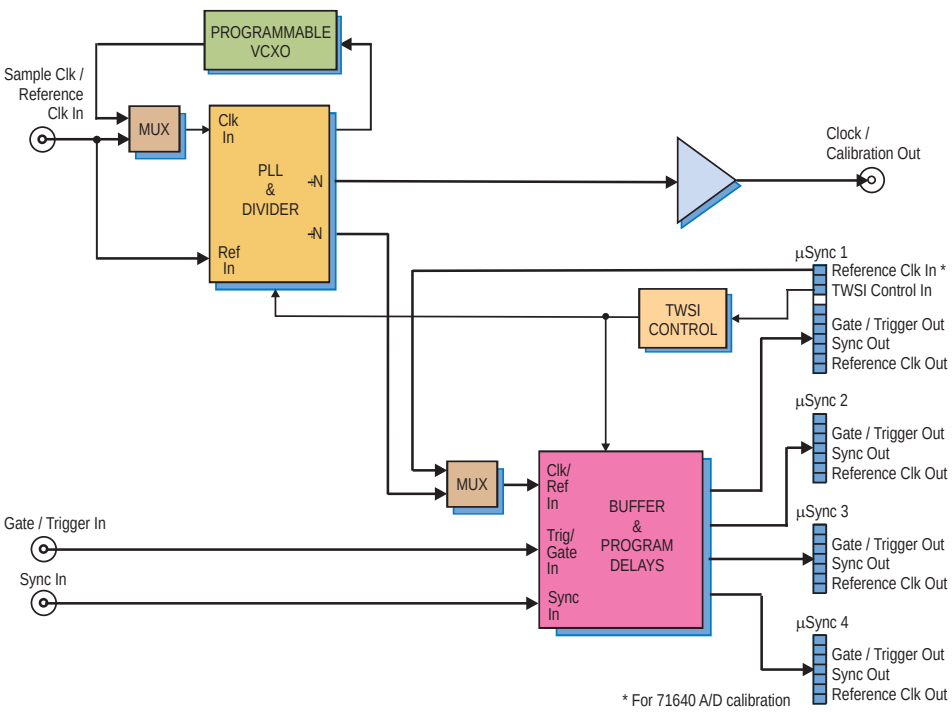
Clock Signals

The 7192 can accept a user supplied external clock on its front panel MMCX connector. As an alternative to the external clock, the 7192 can use its on-board programmable voltage controlled crystal oscillator (VCXO) as the clock source. The VCXO can operate alone or be locked to a system reference clock signal delivered to the front panel reference clock input.

The external or on-board clock can operate at full rate or be divided and is used to register all sync and gate/trigger signals as well as providing a reference clock to all connected modules. In addition, the clock is available at the Clock Out MMCX as a sample or reference clock for other boards in the system.

Gate and Synchronization Signals

The 7192 features separate inputs for gate/trigger and sync signals. A programmable delay allows the user to make timing adjustments on the gate/trigger and sync signals before they are sent to buffers for output through the µSync output connectors. ➤



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Model 7192

High-Speed Synchronizer and Distribution Board - PMC/XMC

Calibration

The 7192 features a calibration output specifically designed to work with the 71640 or 71740 3.6 GHz A/D module and provide a signal reference for phase adjustment across multiple D/As.

Programming

The 7192 allows programming of operating parameters including: VCXO frequency, clock dividers, and delays that allow the user to make timing adjustments on the gate and sync signals. These adjustments are made before they are sent to buffers for output through the µSync connectors.

The 7192 is programmed via a TWSI control interface on the first µSync connector. The control interface is compatible with the front panel µSync connectors of all high-speed Cobalt and Onyx modules, thereby providing a single cable connection that carries both control and timing signals.

Supported Products

The 7192 supports all high-speed models in the Cobalt family including the 71630 1 GHz A/D and D/A XMC, the 71640 3.6 GHz A/D XMC and the 71670 Four-channel 1.25 GHz, 16-bit D/A XMC. The 7192 will also support high-speed models in the Onyx family as they become available.

Specifications

Front Panel Sample Clock/Reference Input
- **Connector Type:** MMCX
- **Input Impedance:** 50 ohms
- **Input Level:** 0 dBm to +10 dBm, sine wave
- **Sample Clock Frequency:** 100 MHz to 2 GHz
- **Reference Frequency:** 5 to 100 MHz

Front Panel Gate/Trigger & Sync Inputs
- **Connector Type:** MMCX
- **Input Level:** LVTTL

Front Panel µSync Inputs/Outputs
- **Quantity:** 4
- **Connector Type:** 19-pin µHDMI
- **Signal Level:** CML
- **Signals (µSync connector 1):** Reference Clock In, TWSI control In, Reference Clock Out, Gate/Trigger Out, Sync Out
- **Signals (µSync connectors 2–4):** Reference Clock Out, Gate/Trigger Out, Sync Out

Front Panel Clock / Calibration Output
- **Connector Type:** MMCX
- **Output Impedance:** 50 ohms
- **Output Level:** +6 dBm nominal, sine wave
- **Sample Clock Frequency:** 100 MHz to 1.8 GHz

Programmable VCXO:
- **Frequency Ranges:** 10-945 MHz, 970-1134 MHz, and 1213-1417.5 MHz
- **Tuning Resolution:** 32 bits
- **Unlocked Accuracy:** ±20 ppm

PLL, Divider & Jitter Cleaner
- **Type:** Texas Instruments CDCM7005
- **Frequency Dividers:** 1, 2, 3, 4, 6, 8 and 16

PMC/XMC Interface: Power only on PMC P1 or XMC P15

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard PMC module, 2.91 in. x 5.87 in.

Ordering Information

Model	Description
7192	High-Speed Synchronizer and Distribution Board - PMC/XMC

Accessories

4 ea. 18" µSync cables are supplied; additional cables may be ordered:

2192-018 µSync cable - 18"

2192-036 µSync cable - 36"

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New!

Models 7292, 7492 and 7392

High-Speed Synchronizer and Distribution Board - 3U/6U cPCI

Model 7392 *Model 7492*

ReadyFlow Board Support Package

Features

- Synchronizes four or eight separate high-speed Cobalt or Onyx I/O boards
- Synchronizes sampling and data acquisition for multichannel systems
- Synchronizes gating and triggering functions
- Clock rates up to 1.8 GHz
- Front panel MMCX connectors for input signals
- Front panel µSync connectors compatible with a range of Pentek Cobalt and Onyx boards

General Information

These High-Speed Synchronizer and Distribution cPCI Boards synchronize multiple Pentek Cobalt or Onyx boards within a system. Thsy enable synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP, and software radio applications.

Up to eight boards can be synchronized using the 7492, with each receiving a common clock along with timing signals that can be used for synchronizing, triggering and gating functions.

Input Signals

These models provide three or six front panel MMCX connectors to accept input signals from external sources: one or two for clock, one or two for gate or trigger and one or two for synchronization signals. Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. In addition to the MMCX connector, a reference clock can be accepted through the front panel µSync output connectors, allowing a single Cobalt or Onyx board to generate the clock for all subsequent boards in the system.

Output Signals

These models provide up to eight front panel µSync output connectors, compatible with a range of high-speed Pentek Cobalt and Onyx boards. The µSync signals include reference clocks, gate/triggers and sync signals and are distributed through matched cables, simplifying system design.

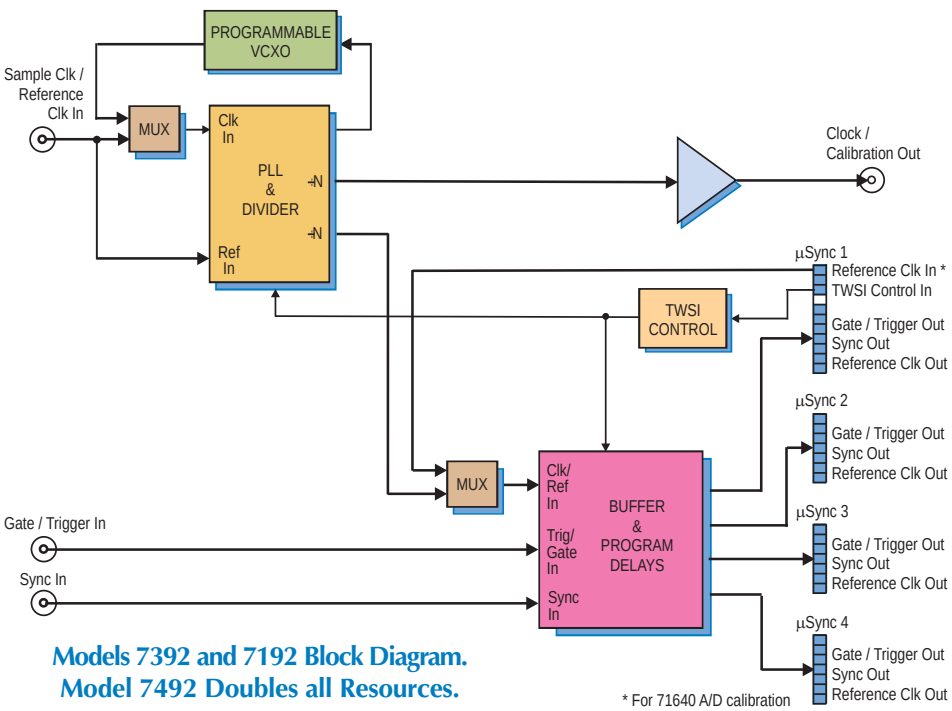
Clock Signals

These modles can accept one or two user supplied external clocks on front panel MMCX connectors. As an alternative to the external clock, they can use on-board programmable voltage controlled crystal oscillators(VCXOs) as the clock sources. The VCXOs can operate alone or be locked to a system reference clock signal delivered to the front panel reference clock inputs.

The external or on-board clocks can operate at full rate or be divided and is used to register all sync and gate/trigger signals as well as providing reference clocks to all connected boards. In addition, the clocks are available at the Clock Out MMCX as sample or reference clocks for other boards in the system.

Gate and Synchronization Signals

These models feature separate inputs for gate/trigger and sync signals. Programmable delays allow the user to make timing adjustments on the gate/trigger and sync signals before they are sent to buffers for output through the µSync output connectors. ➤



Models 7392 and 7192 Block Diagram.
Model 7492 Doubles all Resources.

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Models 7292, 7492 and 7392

High-Speed Synchronizer and Distribution Board - 3U/6U cPCI

Calibration

These models feature a calibration output specifically designed to work with the 72640, 74640 and 73640 or 72740, 74740 and 73740 3.6 GHz A/D board and provide a signal reference for phase adjustment across multiple D/As.

Programming

These models allow programming of operating parameters including: VCXO frequency, clock dividers, and delays that allow the user to make timing adjustments on the gate and sync signals. These adjustments are made before they are sent to buffers for output through the µSync connectors.

These models are programmed via a TWSI control interface on the first µSync connector. The control interface is compatible with the front panel µSync connectors of all high-speed Cobalt and Onyx boards, thereby providing a single cable connection that carries both control and timing signals.

Supported Products

These models support all high-speed models in the Cobalt family including the 72630, 74630 and 73630 1 GHz A/D and D/A cPCI boards; the 72640, 74640 and 73640 3.6 GHz A/D cPCI boards; and the 72670, 74670 and 73670 Four-channel 1.25 GHz, 16-bit D/A cPCI boards. They will also support high-speed models in the Onyx family as they become available.

Specifications

Front Panel Sample Clock/Reference Input
- **Connector Type:** MMCX
- **Input Impedance:** 50 ohms
- **Input Level:** 0 dBm to +10 dBm, sine wave
- **Sample Clock Frequency:** 100 MHz to 2 GHz
- **Reference Frequency:** 5 to 100 MHz

Front Panel Gate/Trigger & Sync Inputs
- **Connector Type:** MMCX
- **Input Level:** LVTTL

Front Panel µSync Inputs/Outputs
- **Quantity:** 4 or 8
- **Connector Type:** 19-pin µHDMI
- **Signal Level:** CML
- **Signals (µSync connector 1):** Reference Clock In, TWSI control In, Reference Clock Out, Gate/Trigger Out, Sync Out
- **Signals (µSync connectors 2–4):** Reference Clock Out, Gate/Trigger Out, Sync Out

Front Panel Clock / Calibration Output
- **Connector Type:** MMCX
- **Output Impedance:** 50 ohms
- **Output Level:** +6 dBm nominal, sine wave
- **Sample Clock Frequency:** 100 MHz to 1.8 GHz

Programmable VCXOs:
- **Frequency Ranges:** 10-945 MHz, 970-1134 MHz, and 1213-1417.5 MHz
- **Tuning Resolution:** 32 bits
- **Unlocked Accuracy:** ±20 ppm

PLL, Divider & Jitter Cleaner
- **Type:** Texas Instruments CDCM7005
- **Frequency Dividers:** 1, 2, 3, 4, 6, 8 and 16

PCI Interface
- **PCI Bus:** 32-bit, 66 MHz (supports 33 MHz), power only

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard 3U or 6U cPCI board

Ordering Information

Model	Description
7292	High-Speed Synchronizer and Distribution Board - 6U cPCI
7492	High-Speed Synchronizer and Distribution Board - 6U cPCI
7392	High-Speed Synchronizer and Distribution Board - 3U cPCI

Accessories

4 ea. 18" µSync cables are supplied with Models 7292 and 7392;

8 ea. 18" µSync cables are supplied with Model 7492;

additional cables may be ordered:

2192-018 µSync cable - 18"

2192-036 µSync cable - 36"

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New!

Model 7892

High-Speed Synchronizer and Distribution Board - PCIe

ReadyFlow Board Support Package

Features

- Synchronizes up to four separate high-speed Cobalt or Onyx I/O boards
- Synchronizes sampling and data acquisition for multichannel systems
- Synchronizes gating and triggering functions
- Clock rates up to 1.8 GHz
- Front panel MMCX connectors for input signals
- Front panel µSync connectors compatible with a range of Pentek Cobalt and Onyx boards

General Information

The Model 7892 High-Speed Synchronizer and Distribution PCIe Board synchronizes multiple Pentek Cobalt or Onyx boards within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP, and software radio applications.

Up to four boards can be synchronized using the 7892, with each receiving a common clock along with timing signals that can be used for synchronizing, triggering and gating functions.

Input Signals

Model 7892 provides three front panel MMCX connectors to accept input signals from external sources: one for clock, one for gate or trigger and one for a synchronization signal. Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. In addition to the MMCX connector, a reference clock can be accepted through the first front panel µSync output connector, allowing a single Cobalt or Onyx board to generate the clock for all subsequent boards in the system.

Output Signals

The 7892 provides four front panel µSync output connectors, compatible with a range of high-speed Pentek Cobalt and Onyx boards. The µSync signals include a reference clock, gate/trigger and sync signals and are distributed through matched cables, simplifying system design.

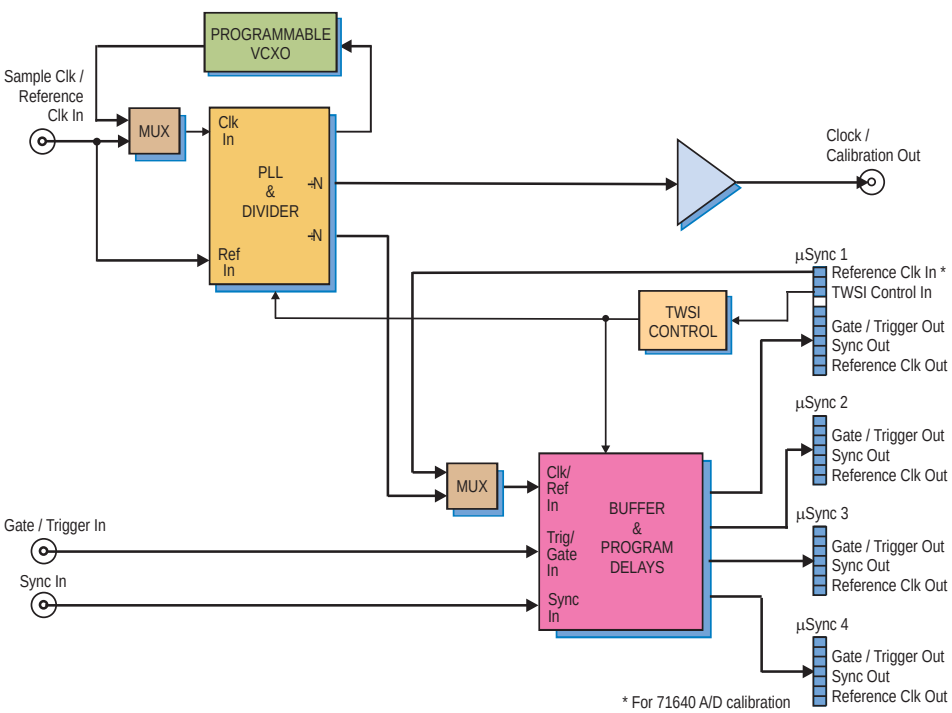
Clock Signals

The 7892 can accept a user supplied external clock on its front panel MMCX connector. As an alternative to the external clock, the 7892 can use its on-board programmable voltage controlled crystal oscillator (VCXO) as the clock source. The VCXO can operate alone or be locked to a system reference clock signal delivered to the front panel reference clock input.

The external or on-board clock can operate at full rate or be divided and is used to register all sync and gate/trigger signals as well as providing a reference clock to all connected boards. In addition, the clock is available at the Clock Out MMCX as a sample or reference clock for other boards in the system.

Gate and Synchronization Signals

The 7892 features separate inputs for gate/trigger and sync signals. A programmable delay allows the user to make timing adjustments on the gate/trigger and sync signals before they are sent to buffers for output through the µSync output connectors. ➤



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Model 7892 — High-Speed Synchronizer and Distribution Board - PCIe

Calibration

The 7892 features a calibration output specifically designed to work with the 78640 or 78740 3.6 GHz A/D board and provide a signal reference for phase adjustment across multiple D/As.

Programming

The 7892 allows programming of operating parameters including: VCXO frequency, clock dividers, and delays that allow the user to make timing adjustments on the gate and sync signals. These adjustments are made before they are sent to buffers for output through the µSync connectors.

The 7892 is programmed via a TWSI control interface on the first µSync connector. The control interface is compatible with the front panel µSync connectors of all high-speed Cobalt and Onyx boards, thereby providing a single cable connection that carries both control and timing signals.

Supported Products

The 7892 supports all high-speed models in the Cobalt family including the 78630 1 GHz A/D and D/A x8 PCIe, the 78640 3.6 GHz A/D x8 PCIe and the 78670 Four-channel 1.25 GHz, 16-bit D/A x8 PCIe. The 7892 will also support high-speed models in the Onyx family as they become available.

Specifications

Front Panel Sample Clock/Reference Input
- **Connector Type:** MMCX
- **Input Impedance:** 50 ohms
- **Input Level:** 0 dBm to +10 dBm, sine wave
- **Sample Clock Frequency:** 100 MHz to 2 GHz
- **Reference Frequency:** 5 to 100 MHz

Front Panel Gate/Trigger & Sync Inputs
- **Connector Type:** MMCX
- **Input Level:** LVTTL

Front Panel µSync Inputs/Outputs
- **Quantity:** 4
- **Connector Type:** 19-pin µHDMI
- **Signal Level:** CML
- **Signals (µSync connector 1):** Reference Clock In, TWSI control In, Reference Clock Out, Gate/Trigger Out, Sync Out
- **Signals (µSync connectors 2–4):** Reference Clock Out, Gate/Trigger Out, Sync Out

Front Panel Clock / Calibration Output
- **Connector Type:** MMCX
- **Output Impedance:** 50 ohms
- **Output Level:** +6 dBm nominal, sine wave
- **Sample Clock Frequency:** 100 MHz to 1.8 GHz

Programmable VCXO:
- **Frequency Ranges:** 10-945 MHz, 970-1134 MHz, and 1213-1417.5 MHz
- **Tuning Resolution:** 32 bits
- **Unlocked Accuracy:** ±20 ppm

PLL, Divider & Jitter Cleaner
- **Type:** Texas Instruments CDCM7005
- **Frequency Dividers:** 1, 2, 3, 4, 6, 8 and 16

PCI Express Interface
- **PCIe Bus:** x4 or x8, power only

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Half length PCIe card, 4.38 in. x 7.13 in.

Ordering Information

Model	Description
7892	High-Speed Synchronizer and Distribution Board - PCIe

Accessories

4 ea. 18" µSync cables are supplied; additional cables may be ordered:

2192-018	µSync cable - 18"
2192-036	µSync cable - 36"

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New!

Model 5392

High-Speed Synchronizer and Distribution Board - 3U VPX

Model 5392 COTS (left) and rugged version

ReadyFlow Board Support Package

Features

- Synchronizes up to four separate high-speed Cobalt or Onyx I/O boards
- Synchronizes sampling and data acquisition for multichannel systems
- Synchronizes gating and triggering functions
- Clock rates up to 1.8 GHz
- Front panel MMCX connectors for input signals
- Front panel µSync connectors compatible with a range of Pentek Cobalt and Onyx boards

General Information

The Model 5392 High-Speed Synchronizer and Distribution 3U VPX Board synchronizes multiple Pentek Cobalt or Onyx boards within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP, and software radio applications.

Up to four boards can be synchronized using the 5392, with each receiving a common clock along with timing signals that can be used for synchronizing, triggering and gating functions.

Input Signals

Model 5392 provides three front panel MMCX connectors to accept input signals from external sources: one for clock, one for gate or trigger and one for a synchronization signal. Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. In addition to the MMCX connector, a reference clock can be accepted through the first front panel µSync output connector, allowing a single Cobalt or Onyx board to generate the clock for all subsequent boards in the system.

Output Signals

The 5392 provides four front panel µSync output connectors, compatible with a range of high-speed Pentek Cobalt and Onyx boards. The µSync signals include a reference clock, gate/trigger and sync signals and are distributed through matched cables, simplifying system design.

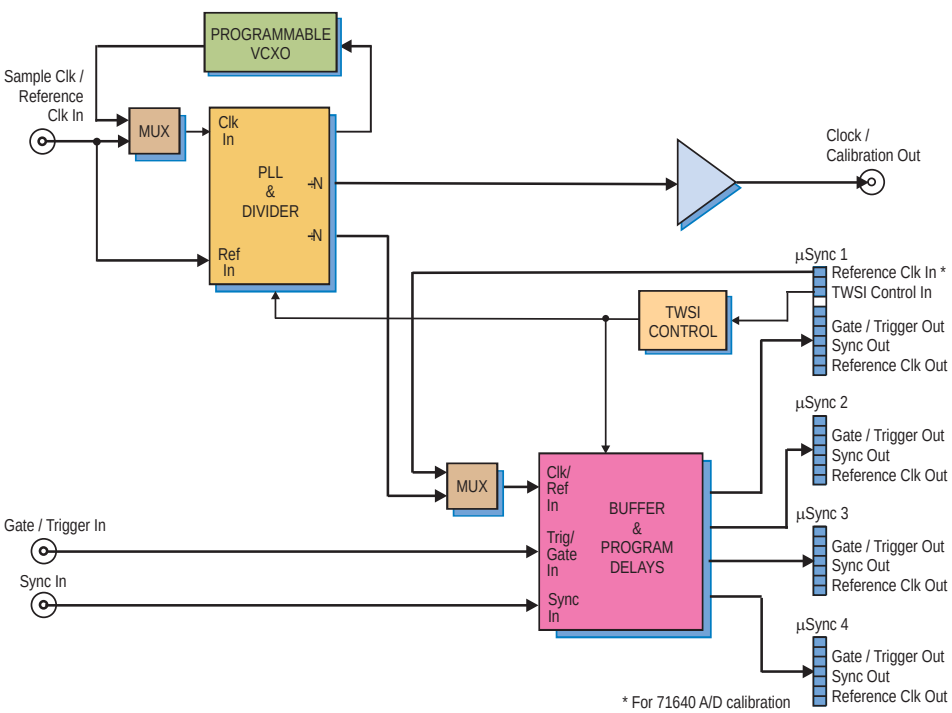
Clock Signals

The 5392 can accept a user supplied external clock on its front panel MMCX connector. As an alternative to the external clock, the 5392 can use its on-board programmable voltage controlled crystal oscillator (VCXO) as the clock source. The VCXO can operate alone or be locked to a system reference clock signal delivered to the front panel reference clock input.

The external or on-board clock can operate at full rate or be divided and is used to register all sync and gate/trigger signals as well as providing a reference clock to all connected boards. In addition, the clock is available at the Clock Out MMCX as a sample or reference clock for other boards in the system.

Gate and Synchronization Signals

The 5392 features separate inputs for gate/trigger and sync signals. A programmable delay allows the user to make timing adjustments on the gate/trigger and sync signals before they are sent to buffers for output through the µSync output connectors. ➤



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Model 5392 — High-Speed Synchronizer and Distribution Board - 3U VPX

Calibration

The 5392 features a calibration output specifically designed to work with the 53640 or 53740 3.6 GHz A/D board and provide a signal reference for phase adjustment across multiple D/As.

Programming

The 5392 allows programming of operating parameters including: VCXO frequency, clock dividers, and delays that allow the user to make timing adjustments on the gate and sync signals. These adjustments are made before they are sent to buffers for output through the µSync connectors.

The 5392 is programmed via a TWSI control interface on the first µSync connector. The control interface is compatible with the front panel µSync connectors of all high-speed Cobalt and Onyx boards, thereby providing a single cable connection that carries both control and timing signals.

Supported Products

The 5392 supports all high-speed models in the Cobalt family including the 53630 1 GHz A/D and D/A 3U VPX, the 53640 3.6 GHz A/D x3U VPX and the 53670 Four-channel 1.25 GHz, 16-bit D/A 3U VPX. The 5392 will also support high-speed models in the Onyx family as they become available.

Specifications

Front Panel Sample Clock/Reference Input
- **Connector Type:** MMCX
- **Input Impedance:** 50 ohms
- **Input Level:** 0 dBm to +10 dBm, sine wave
- **Sample Clock Frequency:** 100 MHz to 2 GHz
- **Reference Frequency:** 5 to 100 MHz

Front Panel Gate/Trigger & Sync Inputs
- **Connector Type:** MMCX
- **Input Level:** LVTTL

Front Panel µSync Inputs/Outputs
- **Quantity:** 4
- **Connector Type:** 19-pin µHDMI
- **Signal Level:** CML
- **Signals (µSync connector 1):** Reference Clock In, TWSI control In, Reference Clock Out, Gate/Trigger Out, Sync Out
- **Signals (µSync connectors 2–4):** Reference Clock Out, Gate/Trigger Out, Sync Out

Front Panel Clock / Calibration Output
- **Connector Type:** MMCX
- **Output Impedance:** 50 ohms
- **Output Level:** +6 dBm nominal, sine wave
- **Sample Clock Frequency:** 100 MHz to 1.8 GHz

Programmable VCXO:
- **Frequency Ranges:** 10-945 MHz, 970-1134 MHz, and 1213-1417.5 MHz
- **Tuning Resolution:** 32 bits
- **Unlocked Accuracy:** ±20 ppm

PLL, Divider & Jitter Cleaner
- **Type:** Texas Instruments CDCM7005
- **Frequency Dividers:** 1, 2, 3, 4, 6, 8 and 16

PCI Express Interface
- **PCIe Bus:** x4 or x8, power only

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: 3.937 in. x 6.717 in. (100 mm x 170.6 mm)

Ordering Information

Model	Description
5392	High-Speed Synchronizer and Distribution Board - 3U VPX

Accessories

4 ea. 18" µSync cables are supplied; additional cables may be ordered:

2192-018	µSync cable - 18"
2192-036	µSync cable - 36"

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New!

Model 7893

System Synchronizer and Distribution Board - PCIe

ReadyFlow Board Support Package

Features

- Synchronizes up to eight separate Cobalt or Onyx boards
- Up to eight 7893s can be linked together to synchronize up to 64 boards
- Synchronizes sampling, data acquisition and playback for multichannel systems
- Synchronizes gating and triggering functions
- On-board programmable sample clock generator
- Output clock rates up to 800 MHz
- Front panel SMA connectors for TTL input signals and clock outputs
- Single-slot PCIe format

General Information

Model 7893 System Synchronizer and Distribution Board synchronizes multiple Pentek Cobalt and Onyx boards within a system. It enables synchronous sampling, playback and timing for a wide range of multichannel high-speed data acquisition, DSP and software radio applications.

Up to eight boards can be synchronized using the 7893, each receiving a common clock up to 800 MHz along with timing signals that can be used for synchronizing, triggering and gating functions.

For larger systems, up to eight 7893s can be linked together to provide synchronization for up to 64 Cobalt or Onyx boards.

Input Signals

The Model 7893 provides four front panel SMA connectors to accept LVTTL input signals from external sources: two for Sync/PPS and one for Gate/Trigger. In addition to the synchronization signals, a front panel SMA connector accepts sample clocks up to 800 MHz or, in an alternate mode, accepts a 10 MHz reference clock to lock an on-board VCXO sample clock source.

The 7893 also accepts the 26-pin Timing Bus connector used on Cobalt and Onyx boards. This input allows a single Cobalt or Onyx board to generate the timing and clock signals for the 7893 for distribution of up to eight additional boards. This input can also be used to link multiple 7893's for larger systems.

Output Signals

The 7893 provides eight timing bus output connectors for distributing all needed timing and clock signals to the front panels of Cobalt and Onyx boards via ribbon cables. The 7893 locks the Gate/Trigger and Sync/PPS signals to the system's sample clock. The 7893 also provides four front panel SMA connectors for distributing sample clocks to other boards in the system.

Clock Signals

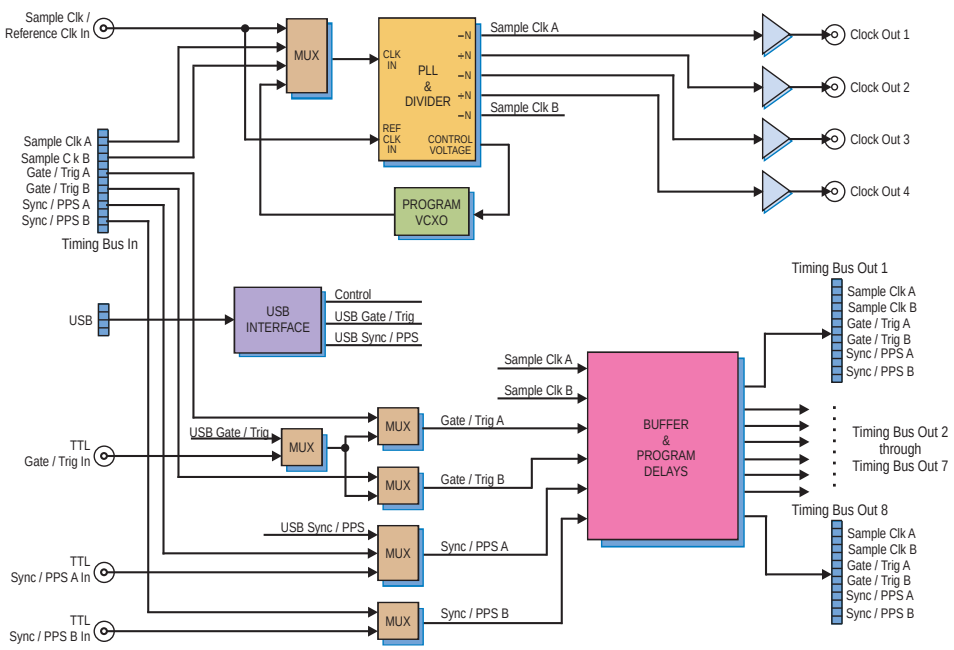
The 7893 can accept a clock from either the front panel SMA connector or from the timing bus input connector. In addition, the board is equipped with a programmable on-board VCXO clock generator which can free run or be locked to a user supplied, 10 MHz typical, system reference. In all cases, the sample clock can be divided by 1, 2, 4, 8 or 16 prior to distribution to the Clock Out SMAs or the timing bus output connectors.

USB Interface

The 7893 is programmed via a USB interface. In addition to status and control, the USB interface can be used to generate Gate/Trigger and Sync/PPS signals for distribution to all connected boards.

Physical Characteristics

The 7893 is a single-slot PCIe size board which can be mounted in any PCI or PCIe slot. The board receives power from a standard six-pin PCIe power connector and uses the PCI or PCIe slot solely for physical mounting, with no electrical connections. ➤



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Model 7893 System Synchronizer and Distribution Board - PCIe

➤ Supported Products

The 7893 supports a wide range of products in the Cobalt family including the 78620 and 78621 three-channel A/D, 200 MHz transceivers, the 78650 and 78651 two-channel A/D, 500 MHz transceivers, the 78660, 78661 and 78662 four-channel 200 MHz A/Ds, and the 78690 L-Band RF Tuner. The 7893 also supports the Onyx 78760 four-channel 200 MHz A/D and will support all complementary models in the Onyx family as they become available.

Specifications

Sample Clock/Reference Clock Input
- **Type:** Front panel female SMC connector
- **Signal:** Sine wave, 0 to +10 dBm, AC-coupled, 50 ohms, accepts 10 to 800 MHz sample clock or 4 to 180 MHz PLL system reference, typically 10 MHz

TTL Gate/Trigger Input
- **Type:** Front panel female SMC connector
- **Signal:** LVTTL
- **Function:** Programmable functions include gate and trigger

TTL Sync/PPS Input A
- **Type:** Front panel female SMC connector
- **Signal:** LVTTL
- **Function:** Programmable functions include sync and PPS

TTL Sync/PPS Input B
- **Type:** Front panel female SMC connector
- **Signal:** LVTTL
- **Function:** Programmable functions include sync and PPS

Timing Bus In
- **Type:** One rear 26-pin connector
- **Signals:** LVPECL bus includes: Sample Clock A & B In, Gate/Trigger A & B In, and Sync/PPS A & B In

Clock Synthesizer
- **Clock Source:** Selectable from on-board programmable VCXO (10 to 800 MHz), front panel external clock or LVPECL timing bus
- **Synchronization:** VCXO can be locked to an external 4 to 180 MHz PLL system reference (front panel Reference Clock Input), typically 10 MHz
- **Clock Dividers**: External clock or VCXO can be divided by 1, 2, 4, 8, or 16 for each of five on-board clock buses.

Sample Clock Output
- **Type:** Four front panel female SMC connectors, each can be independently divided
- **Output Level:** +9 dBm, nominal, sine wave

Timing Bus Out
- **Type:** Eight rear 26-pin connectors
- **Signals:** LVPECL bus includes: Sample Clock A & B Out, Gate/Trigger A & B Out, and Sync/PPS A & B Out

Control: Rear USB input for connecting to motherboard on-board USB 8-pin header

Power: Rear 8-pin connector compatible with PCIe power connectors

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Half-length PCIe card, 4.38 in. x 7.13 in.

Ordering Information

Model	Description
7893	System Synchronizer and Distribution Board- PCIe

Accessories

2891	Timing Bus Cables

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Model 9190 Clock and Sync Generator for I/O Modules

Features

- Synchronizes up to 80 I/O modules
- Synchronizes sampling and data acquisition for multichannel systems
- Synchronizes gating and triggering functions
- Synchronizes local oscillator phase, decimation phase and frequency switching for multichannel digital receivers and upconverters
- Clock rates up to 105 MHz
- Supports most popular I/O modules
- Front panel SMA connectors for external clock and timing signal inputs and outputs
- 19-inch wide, 1.75 in. high rack-mount chassis with integral AC line power supply
- Flexible cable installation supports many different system configurations

General Information

Model 9190 Clock and Sync Generator synchronizes multiple Pentek I/O modules within a system to provide synchronous sampling and timing for a wide range of high-speed, multichannel data acquisition, DSP and software radio applications. Up to 80 I/O modules can be driven from the Model 9190, each receiving a common clock and up to five different timing signals which can be used for synchronizing, triggering and gating functions.

Input Signals

Clock and timing signals can come from six front panel SMA user inputs or from one I/O module set to act as the timing signal master. (In this case, the master I/O module will not be synchronous with the slave modules due to delays through the 9190.) Alternately, the master clock can come from a socketed, user-replaceable crystal oscillator within the 9190.

Supported Products

Model 9190 currently supports VIM Models 6210, 6211, 6216, 6228, 6229, 6230, 6231, 6232, 6235, 6236; the PMC Models 7131, 7140, 7141, 7142 and 7150; the PCI Models 7631A, 7640, 7641, 7642 and 7650; and the cPCI Models 7231, 7331, 7240, 7340, 7241, 7341, 7242, 7342 and 7350. Contact us for an up-to-date list of supported modules.

Output Signals

The front panel clock and sync connectors in the list of supported modules fall into two classes, thus requiring two types of front panel cable. The first type uses a 26-pin connector (for the 621x series, the 6229, the 7x31, 7x40 and 7x42 series) delivering the clock and four timing signals. The second type uses a 36-pin connector (for the 623x series) delivering the clock and five timing signals.

Either cable type can be installed in any of the 80 positions of the Model 9190, however, systems with mixed types of I/O modules may not have all functions supported. Contact the factory for assistance with your specific configuration.

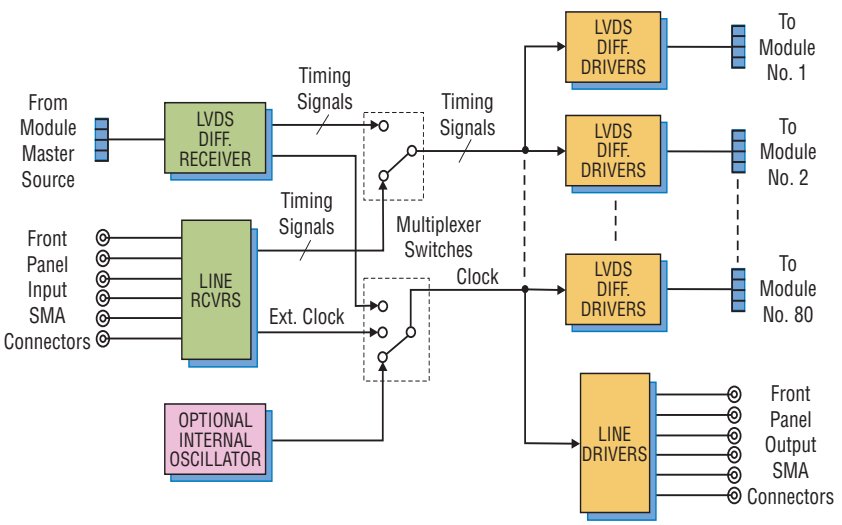
Buffered versions of the clock and five timing signals are also available as outputs on the 9190's front panel SMA connectors.

Physical Characteristics

Model 9190 is housed in a line-powered, 1.75 in. high metal chassis suitable for mounting in a standard 19 in. equipment rack, either above or below the cage holding the I/O modules.

Separate cable assemblies extend from openings in the front panel of the 9190 to the front panel clock and sync connectors of each I/O module. Mounted between two standard rack-mount card cages, Model 9190 can drive a maximum of 80 clock and sync cables, 40 to the card cage above and 40 to the card cage below. Fewer cables may be installed for smaller systems.

Due to the numerous configuration possibilities allowed by the 9190, Pentek configuration services are required with its purchase.



Ordering Information

Model	Description
9190	Clock and Sync Generator
Options:	
-019	64 MHz internal oscillator
-040	40-Channel version

New!

Model 9192

Rackmount High-Speed System Synchronizer Unit

General Information

Model 9192 Rackmount High-Speed System Synchronizer Unit synchronizes multiple Pentek Cobalt or Onyx modules within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP, and software radio applications.

Up to twelve boards can be synchronized using the 9192, each receiving a common clock along with timing signals that can be used for synchronizing, triggering and gating functions.

Input Signals

Model 9192 provides four rear panel SMA connectors to accept input signals from external sources: two for clock, one for gate or trigger and one for a synchronization signal. Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. In addition to the SMA connector, a reference clock can be accepted through the first rear panel µSync output connector, allowing a single Cobalt or Onyx board to generate the clock for all subsequent boards in the system.

Output Signals

The 9192 provides four rear panel µSync output connectors, compatible with a range of high-speed Pentek Cobalt and Onyx boards. The µSync signals include a reference clock, gate/trigger and sync signals and are distributed through matched cables, simplifying system design.

Clock Signals

The 9192 can accept a user supplied external clock on its rear panel SMA connector. As an alternative to the external clock, the 9192 can use its on-board programmable voltage controlled crystal oscillator (VCXO) as the clock source. The VCXO can operate alone or be locked to a system reference clock signal delivered to the rear panel reference clock input.

The on-board or external clock can operate at full rate or can be divided and used to register all sync and gate/trigger signals as well as providing a reference clock to all connected boards. In addition, the clock is available at twelve Clock Out SMAs as a sample or reference clock for other boards in the system.

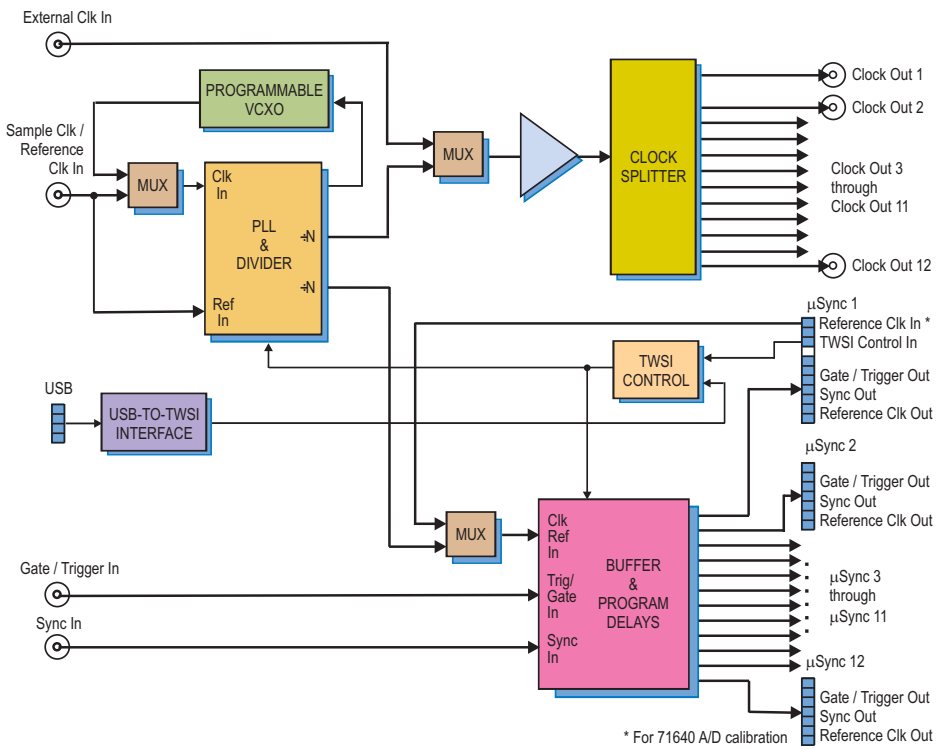
Gate and Synchronization Signals

The 9192 features separate inputs for gate/trigger and sync signals. A programmable delay allows the user to make timing adjustments on the gate/trigger and sync signals before they are sent to buffers for output through the µSync output connectors. ➤

ReadyFlow Board Support Package

Features

- Synchronizes up to twelve separate high-speed Cobalt or Onyx I/O modules
- Synchronizes sampling and data acquisition for multichannel systems
- Synchronizes gating and triggering functions
- Clock rates up to 1.8 GHz
- Rear panel SMA connectors for input signals
- Rear panel µSync connectors compatible with a range of Pentek Cobalt and Onyx modules



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Model 9192

Rackmount High-Speed System Synchronizer Unit

➤ Calibration

The 9192 features twelve calibration outputs specifically designed to work with the 71640 or 71740 3.6 GHz A/D module and provide a signal reference for phase adjustment across multiple D/As

Programming

The 9192 allows programming of operation parameters including: VCXO frequency, clock dividers, and delays that allow the user to make timing adjustments on the gate and sync signals. These adjustments are made before they are sent to buffers for output through the µSync connectors.

The 9192 is programmed via a rear panel USB connector or a TWSI control interface on the first µSync connector. The control interface is compatible with the front panel µSync connectors of all high-speed Cobalt and Onyx modules, thereby providing a single cable connection that carries both control and timing signals.

Supported Products

The 9192 supports all high-speed models in the Cobalt family including the 71630 1 GHz A/D and D/A XMC, the 71640 3.6 GHz A/D XMC and the 71670 Four-channel 1.25 GHz, 16-bit D/A XMC. The 9192 will also support high-speed models in the Onyx family as they become available.

Specifications

Front Panel Sample Clock / Reference Input
- **Connector Type:** SMA
- **Input Impedance:** 50 ohms
- **Input Level:** 0 dBm to +10 dBm, sine wave
- **Sample Clock Frequency:** 100 MHz to 2 GHz
- **Reference Frequency:** 5 to 100 MHz

Rear Panel Gate/Trigger & Sync Inputs
- **Connector Type:** SMA
- **Input Level:** LVTTL

Rear Panel µSync Inputs/Outputs
- **Quantity:** 12
- **Connector Type:** 19-pin µHDMI
- **Signal Level:** CML
- **Signals (µSync connector 1):** Reference Clock In, TWSI control In, Reference Clock Out, Gate/Trigger Out, Sync Out
- **Signals (µSync connectors 2-12):** Reference Clock Out, Gate/Trigger Out, Sync Out

Rear Panel Clock / Calibration Outputs
- **Quantity:** 12
- **Connector Type:** SMA
- **Output Impedance:** 50 ohms
- **Output Level:** +6 dBm nominal at 1400 MHz, sine wave
- **Sample Clock Frequency:** 100 MHz to 1.8 GHz

Programmable VCXO:
- **Frequency Ranges:** 10-945 MHz, 970-1134 MHz, and 1213-1417.5 MHz
- **Tuning Resolution:** 32 bits
- **Unlocked Accuracy:** ±20 ppm

PLL, Divider & Jitter Cleaner
- **Type:** Texas Instruments CDCM7005
- **Frequency Dividers:** 1, 2, 3, 4, 6, 8 and 16

Power: 120VAC

Environmental
- **Operating Temp:** 0° to 50° C
- **Storage Temp:** –20° to 90° C
- **Relative Humidity:** 0 to 95%, non-cond.

Size: Standard 1U Rackmount, 19 in. x 1.75 in.

Ordering Information

Model	Description
9192	Rackmount High-Speed System Synchronizer Unit

Accessories

12 ea. 18" µSync cables are supplied; additional cables may be ordered:

2192-018 µSync cable - 18"

2192-036 µSync cable - 36"

Specifications are subject to change without notice.

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Customer Information

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International orders may be placed with us, or with our authorized distributor in your country. They have pricing and availability information and they will be pleased to assist you.

Prices and Price Quotations

All prices are F.O.B. factory in U.S. dollars. Shipping charges and applicable import, federal, state or local taxes, are paid by the purchaser.

We're glad to respond to your request for price quotation — just contact the corporate office, or your local representative. Price and delivery quotations are valid for 30 days, unless otherwise stated.

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Terms are Net 30 days for accounts with established credit; until credit is established, we require prepayment, or will ship C.O.D.

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All orders placed with Pentek are considered binding and are subject to cancellation charges. Hardware products included in this catalog may be returned within 30 days after receipt, subject to a restocking charge. Before returning a product, please call Customer Service to obtain a Return Material Authorization (RMA) number. Software purchases are final and we cannot allow returns.

Warranty

Pentek warrants its products to conform to published specifications and to be free from defects in materials and workmanship for a period of one year from the date of delivery, when used under normal operating conditions and within the service conditions for which they were furnished.

The obligation of Pentek arising from a warranty claim shall be limited to repairing or, optionally, replacing without charge any product which proves to be defective within the term and scope of the warranty.

Pentek must be notified of the defect or nonconformity within the warranty period. The affected product must be returned with shipping charges and insurance prepaid. Pentek will pay shipping charges for the return of product to buyer, except for products returned from outside of the USA.

Limitations of Warranty

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The warranty does not extend to products that have been damaged by misuse, neglect, improper installation, unauthorized modification, or extreme environmental conditions.

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All Pentek software products (excluding 3rd-party products) include free maintenance and free upgrades for one year. Extended software maintenance is available for one, two, and three years, starting after the first year.

Service and Repair

Before returning a product for service and repair, please contact Customer Service to obtain a Return Material Authorization (RMA) number and have the following information available: model number, serial number, name and address of person returning the product and a description of the problem experienced.

Carefully package the product in its original antistatic material, if it is still available, and ship it to us: prepaid (if within the US) or free domicile DDP (if outside the US). Show the RMA number on the outside of the package and include a written description of the malfunction.

When the work is completed, we will return the product to you free of charge, along with a statement of work done, if under warranty. Out-of-warranty work will be charged on a material and service time basis, and we will be happy to quote you a cost estimate for the repair and return shipping before proceeding.

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