





PENTEK

Software & FPGA Tools

SOFTWARE & FPGA TOOLS

MODEL	DESCRIPTION
4953	Pentek GateFlow® FPGA Design Kit
4994A	Pentek ReadyFlow BSPs for Linux
4995A	Pentek ReadyFlow BSPs for Windows®
4996/4996A	Pentek VxWorks BSPs and Drivers
VxWorks	Wind River Workbench/VxWorks for PowerPC
—	Pentek SystemFlow® Recording Software
4986	Verari Systems Software VSI/Pro for PowerPC
	Customer Information

Click Here for the PRODUCT SELECTOR

Last updated: September 2012

Model 4953

GateFlow FPGA Design Kit for Cobalt and Onyx Products

GateFlow® is Pentek's family of extendable FPGA products. The GateFlow product line includes the *GateFlow FPGA Design Kit* to ease custom algorithm development and the *GateFlow Factory-installed IP Cores* in Pentek FPGA board products.

The Pentek Model 4953 GateFlow FPGA Design Kit provides the user with design information, software files and utilities for extending FPGA functions in these products.

Users can implement a variety of custom preprocessing functions such as convolution, framing, pattern recognition, decompression, FFT, delay, decoding, time stamping, averaging, summation and many more.

For the latest GateFlow information go to: pentek.com/fpga

Using the FPGA Design Kit

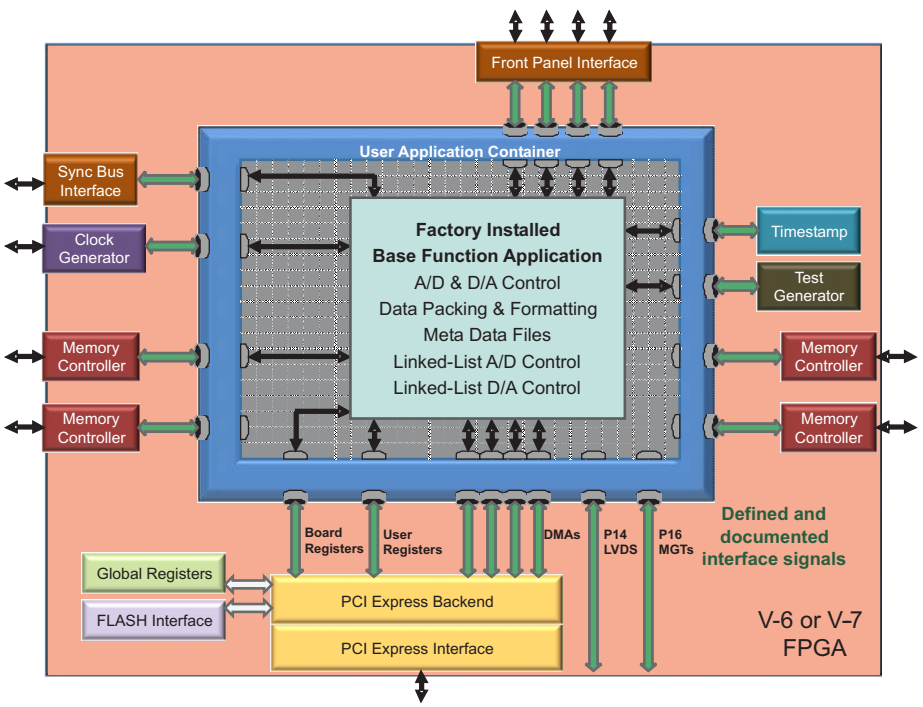
The **GateFlow** FPGA Design Kit allows the user to modify, replace and extend the standard factory-installed functions in the FPGA to incorporate special modes of operation, new control structures, and specialized signal-processing algorithms.

The Cobalt and Onyx architectures configure the FPGA with standard factory-supplied interfaces including memory controllers, DMA engines, A/D and D/A interfaces, timing and synchronization structures, triggering and gating logic, time stamping and header tagging, data formatting engines, and the PCIe interface. These resources are connected to the User Application Container using well-defined ports that present easy-to-use data and control signals, effectively abstracting the lower level details of the hardware.

The User Application Container

Shown below is the FPGA block diagram of a typical Cobalt or Onyx module. The User Application Container holds a collection of different factory-installed IP modules connected to the various interfaces through the standard ports surrounding the container. The specific IP modules for each product are described in further detail in the datasheet of that product.

The GateFlow Design Kit provides a complete Xilinx ISE Foundation Tool project folder containing all the files necessary for the FPGA developer to recompile the entire project with or without any required changes. VHDL source code for each IP module provides excellent examples of how the IP modules work, how they might be modified, and how they might be replaced with custom IP to implement a specific function.



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Model 4953

GateFlow FPGA Design Kit for Other Pentek Products

GateFlow® is Pentek's family of extendable FPGA products. The GateFlow product line includes the *GateFlow FPGA Design Kit* to ease custom algorithm development and the *GateFlow Factory-installed IP Cores* in Pentek FPGA board products.

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For the latest GateFlow information go to: pentek.com/fpga

Using the FPGA Design Kit

The **GateFlow** FPGA Design Kit is intended for the programming of predefined user blocks located in the data flow path specifically reserved for custom applications. These predefined blocks protect users from inadvertently altering base functionality.

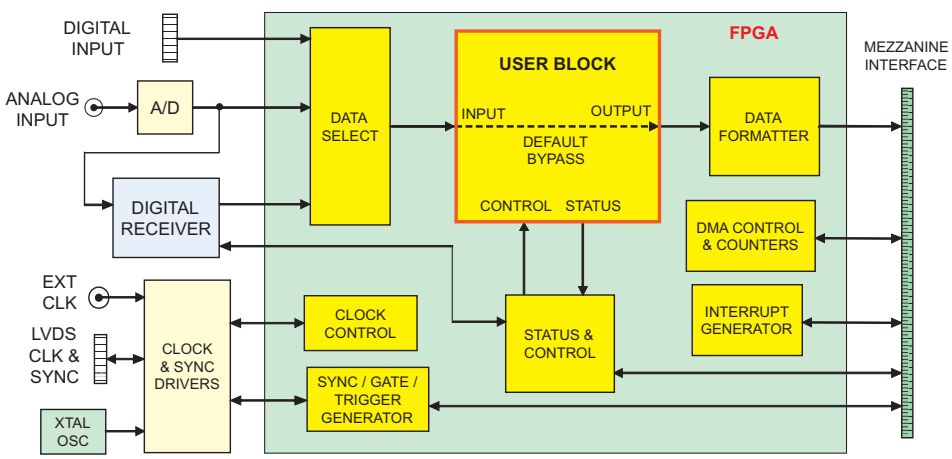
Pentek recommends user programming be limited to the predefined user blocks to maintain base functionality. However, for more complex requirements, sufficient information is supplied in the kit for the user to modify, add to, or replace default board functions if necessary. Default configuration files are included with the Design Kit should it be necessary to restore standard factory configuration.

FPGA Design Kit User Block

Shown below is the block diagram of a typical software radio module. The diagram includes the FPGA and external hardware devices connected to it.

The blocks inside the FPGA are VHDL code modules that handle the standard factory functions and interfaces. The User Block is a VHDL module that sits in the data path with pin definitions for input, output, status, control and clocks.

In the standard Design Kit product, the User Block is configured as a straight wire between the input and output ports. By creating a custom algorithm inside the block that conforms to the pin definition, the user will have a low-risk experience in recompiling and installing the custom code. Since Pentek provides source code for all the modules, changes outside the user block can also be made by the user.



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Xilinx FPGAs in Pentek Products

The charts below show the Xilinx FPGA families as used in the various Pentek board-level products. These products use some FPGA resources to implement standard factory functions as well as installed IP cores.

The charts show the percentage of unused system slices and RAM available to the user for extending the FPGA to include custom algorithms.

Available FPGA Resources for Pentek Hardware

	Xilinx Virtex-II Pro		Xilinx Virtex-4			
	-VP50	-VP70	-FX60	-FX100	-SX55	-LX100
Logic Cells	53,136	74,448	56,880	94,986	55,296	110,592
CLB Slices	23,616	33,088	25,280	42,176	24,576	49,152
CLB Flip-Flops	47,232	66,176	50,560	84,352	49,152	98,304
Max. Block RAM	4,176 k	5,904 k	4,176 k	6,768 k	5,760 k	4,320 k
Multipliers / DSP Blocks	232	328	128	160	512	96
PowerPC Processor Blocks	2	2	2	2	–	–

Pentek Model	Board Type	No. of FPGAs	% Available to User				% Available to User							
			Slices	RAM	Slices	RAM	Slices	RAM	Slices	RAM	Slices	RAM	Slices	RAM
4207	VME/VXS	1	–	–	–	–	38%	71%	61%	82%	–	–	–	–
6251	VIM-2	2	99%	100%	–	–	–	–	–	–	–	–	–	–
6256	VIM-2	2	98%	100%	–	–	–	–	–	–	–	–	–	–
6821	VME/VXS	2	98%	100%	–	–	–	–	–	–	–	–	–	–
6822	VME/VXS	2	98%	100%	–	–	–	–	–	–	–	–	–	–
6826	VME/VXS	1	–	–	75%	72%	–	–	–	–	–	–	–	–
7140*	PMC/XMC	1	55%	72%	–	–	–	–	–	–	–	–	–	–
7141*	PMC/XMC	1	55%	72%	–	–	–	–	–	–	–	–	–	–
7142*	PMC/XMC	2	–	–	–	–	77%	92%	86%	95%	54%	78%	77%	71%

Available FPGA Resources for Pentek Hardware

	Xilinx Virtex-5			Xilinx Virtex-6				
	-SX50T	-SX95T	-LX155T	-LX130T	-LX240T	-LX365T	-SX315T	-SX475T
Logic Cells	52,224	94,208	155,648	128,000	241,152	364,032	314,880	476,160
CLB Slices	8,160	14,720	24,320	20,000	37,680	56,880	49,200	74,400
CLB Flip-Flops	32,640	58,880	97,280	160,000	301,440	455,040	393,600	595,200
Max. Block RAM	4,752 k	8,784 k	7,632 k	9,504 k	14,976 k	14,976 k	25,344 k	36,304 k
Multipliers / DSP Blocks	288	640	128	480	768	576	1,344	2,016
PowerPC Processor Blocks	–	–	–	–	–	–	–	–

Pentek Model	Board Type	No. of FPGAs	% Available to User						% Available to User									
			Slices	RAM	Slices	RAM	Slices	RAM	Slices	RAM	Slices	RAM	Slices	RAM	Slices	RAM	Slices	RAM
7150*	PMC/XMC	2	7%	75%	36%	86%	64%	84%	–	–	–	–	–	–	–	–	–	–
7153*	PMC/XMC	2	N/A	N/A	42%	45%	N/A	N/A	–	–	–	–	–	–	–	–	–	–
7156*	PMC/XMC	2	16%	59%	50%	78%	69%	74%	–	–	–	–	–	–	–	–	–	–
7158*	PMC/XMC	2	16%	59%	50%	78%	69%	74%	–	–	–	–	–	–	–	–	–	–
71620**	XMC	1	–	–	–	–	–	–	68%	75%	83%	82%	TBD	TBD	TBD	TBD	TBD	TBD
71630**	XMC	1	–	–	–	–	–	–	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
71650**	XMC	1	–	–	–	–	–	–	66%	74%	82%	84%	TBD	TBD	86%	90%	TBD	TBD
71660**	XMC	1	–	–	–	–	–	–	69%	75%	83%	85%	TBD	TBD	TBD	TBD	TBD	TBD
71661**	XMC	1	–	–	–	–	–	–	TBD	TBD	43%	67%	TBD	TBD	TBD	TBD	TBD	TBD
71690**	XMC	1	–	–	–	–	–	–	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

***Other form factors:** 72XX = 6U cPCI; 73XX = 3U cPCI; 76XX = PCI; 77XX = Full-Length PCIe; 78XX = Half-Length PCIe; 53XX = 3U VPX
****Cobalt form factors:** 726XX = 6U CPCI (1 XMC); 736XX = 3U cPCI; 746XX = 6U CPCI (2 XMC); 786XX = Half-Length PCIe; 536XX = 3U VPX
%Available to User: Applies to the Processing FPGA(s) of certain products; % Available can vary slightly due to rounding

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Model 4953 GateFlow FPGA Design Kit

Ordering Information

Model	Description
4953	GateFlow FPGA Design Kit

Options:	Supported Product w/ FPGA option
-131-030*	7131 w/ XC2V3000
-140-052*	7140 w/ XC2VP50
-141-052*	7141 w/ XC2VP50
-142-055*	7142 w/ XC4VSX55
-142-060*	7142 w/ XC4VFX60
-142-100*	7142 w/ XC4VFX100
-142-110*	7142 w/ XC4VLX100
-150-083*	7150 w/ XC5VLX155T
-150-084*	7150 w/ XC5VSX50T
-150-085*	7150 w/ XC5VSX95T
-153-085*	7153 w/ XC5VSX95T
-156-083*	7156 w/ XC5VLX155T
-156-084*	7156 w/ XC5VSX50T
-156-085*	7156 w/ XC5VSX95T
-158-083*	7158 w/ XC5VLX155T
-158-084*	7158 w/ XC5VSX50T
-158-085*	7158 w/ XC5VSX95T
-620-061**	71620 w/ XC6VLX130T
-620-062**	71620 w/ XC6VLX240T
-620-063**	71620 w/ XC6VLX365T
-620-064**	71620 w/ XC6VSX315T
-620-065**	71620 w/ XC6VSX475T
-621-061**	71621 w/ XC6VLX130T
-621-062**	71621 w/ XC6VLX240T
-621-063**	71621 w/ XC6VLX365T
-621-064**	71621 w/ XC6VSX315T
-621-065**	71621 w/ XC6VSX475T
-630-061**	71630 w/ XC6VLX130T
-630-062**	71630 w/ XC6VLX240T
-630-063**	71630 w/ XC6VLX365T
-630-064**	71630 w/ XC6VSX315T
-630-065**	71630 w/ XC6VSX475T
-650-061**	71650 w/ XC6VLX130T
-650-062**	71650 w/ XC6VLX240T
-650-063**	71650 w/ XC6VLX365T
-650-064**	71650 w/ XC6VSX315T
-650-065**	71650 w/ XC6VSX475T
-660-061**	71660 w/ XC6VLX130T
-660-062**	71660 w/ XC6VLX240T
-660-063**	71660 w/ XC6VLX365T
-660-064**	71660 w/ XC6VSX315T
-660-065**	71660 w/ XC6VSX475T

Options:	Supported Product w/ FPGA option
-661-061**	71661 w/ XC6VLX130T
-661-062**	71661 w/ XC6VLX240T
-661-063**	71661 w/ XC6VLX365T
-661-064**	71661 w/ XC6VSX315T
-661-065**	71661 w/ XC6VSX475T
-662-061**	71662 w/ XC6VLX130T
-662-062**	71662 w/ XC6VLX240T
-662-063**	71662 w/ XC6VLX365T
-662-064**	71662 w/ XC6VSX315T
-662-065**	71662 w/ XC6VSX475T
-690-061**	71690 w/ XC6VLX130T
-690-062**	71690 w/ XC6VLX240T
-690-063**	71690 w/ XC6VLX365T
-690-064**	71690 w/ XC6VSX315T
-690-065**	71690 w/ XC6VSX475T
-205-010	4205 w/ XC2V1000
-205-030	4205 w/ XC2V3000
-207-060	4207 w/ XC4VFX60
-207-100	4207 w/ XC4VFX100
-228-010	6228 w/ XC2V1000
-228-030	6228 w/ XC2V3000
-230-006	6230 w/ XCV600E
-231-006	6231 w/ XCV600E
-232-006	6232 w/ XCV600E
-235-010	6235 w/ XC2V1000
-235-030	6235 w/ XC2V3000
-236-010	6236 w/ XC2V1000
-236-030	6236 w/ XC2V3000
-250-010	6250 w/ XC2V1000
-250-030	6250 w/ XC2V3000
-251-022	6251 w/ XC2VP20
-251-052	6251 w/ XC2VP50
-256-022	6256 w/ XC2VP20
-256-052	6256 w/ XC2VP50
-821-022	6821 w/ XC2VP20
-821-052	6821 w/ XC2VP50
-822-022	6822 w/ XC2VP20
-822-052	6822 w/ XC2VP50
-826-072	6826 w/ XC2VP70

***Other form factors:** 72XX = 6U cPCI; 73XX = 3U cPCI; 76XX = PCI; 77XX= Full-Length PCIe; 78XX = Half-Length PCIe; 53XX = 3U VPX
****Cobalt form factors:** 726XX = 6U CPCI (1 XMC); 736XX = 3U cPCI; 746XX = 6U CPCI (2 XMC); 786XX = Half-Length PCIe; 536XX = 3U VPX

Example:	Model	Description	Form Factor
	7150	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs	PMC/XMC
	7250	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs	6U cPCI
	7350	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs	3U cPCI
	7650	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs	PCI
	7750	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs	x16 PCIe
	7850	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs	x8 PCIe
	5350	Quad 200 MHz, 16-bit A/D with Virtex-5 FPGAs	3U VPX

Contact Pentek for the latest products and FPGA options.

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Pentek ReadyFlow - Board Support Package for Linux™

General Information

Users of high-performance data acquisition and signal processing boards often find themselves frustrated by the fact that when their new devices are delivered, they are unable to put them to immediate use.

Because these boards are largely software controlled and offer a flexible range of functionality, a certain amount of programming is generally necessary to put the new cards through their paces. Then, if something does not go as planned, there is no way of knowing for sure whether the problem lies with the new code, or with the hardware itself.

To address this issue, Pentek has developed the **ReadyFlow**® BSPs (Board Support Packages) for all its board-level products. These packages:

- Provide a path for quick start-up through application completion
- Allow programming at high, intermediate and low levels to meet various needs
- Are illustrated with numerous examples
- Include complete documentation and definitions of all functions
- Include library and example source code

What's Included in the Package

In general, functions appropriate to the board-level product, such as:

- A "How to" section
  - Build object libraries
  - Compile and link application programs
- C-callable functions
  - Initialization and test
  - Data movement and communications
  - Backplane I/O
  - Mezzanine peripheral I/O
  - Control of board resources
- Utilities
  - Flash memory program loaders

The package contains C-language examples that can be used to demonstrate the capabilities of Pentek products. The examples included provide the answers to most of the questions that occur with first-time users of Pentek products.

These programming examples will also help you get an immediate start on writing your own application without having to reinvent the wheel. They provide sample code that is known to work, giving you, the new user, a means of verifying that your board set is operational.

ReadyFlow Board Support Packages are designed to reduce development time not only during the initial stages, but any time new hardware is added to the system. All packages are built with a consistent style and function-naming convention. Similar parameters on different boards have similar function calls, thereby allowing immediate familiarity with new hardware as it's added further shortening the learning curve.

Command Line Interface

The Command Line Interface is a pre-compiled executable that runs the hardware right out of the box, without the need to write any code.

Specific to the hardware features of the supported board, it allows operating arguments to be entered on the command line for controlling parameters such as: number of channels to enable, clock select, data transfer size, rate divider, interpolation, clock frequency, reference clock source, number of iterations to run the program, etc.

An example command line for a D/A capable hardware module would look like this:

```
C:> dacmode -chan 1 -xfersize 32768
    -loop 100000 -ratediv 2
    -interpolate 4
```

The Command Line Interface can be called from within a larger user application providing a convenient way to control the hardware. Operating parameters can be dynamically changed while the application is running to address changing application conditions.

For command line functions that control data acquisition, the captured data can be saved in a host file or routed to the Signal Analyzer. ➤

For the latest list of boards supported with ReadyFlow, visit our website at:
www.pentek.com/readyflow

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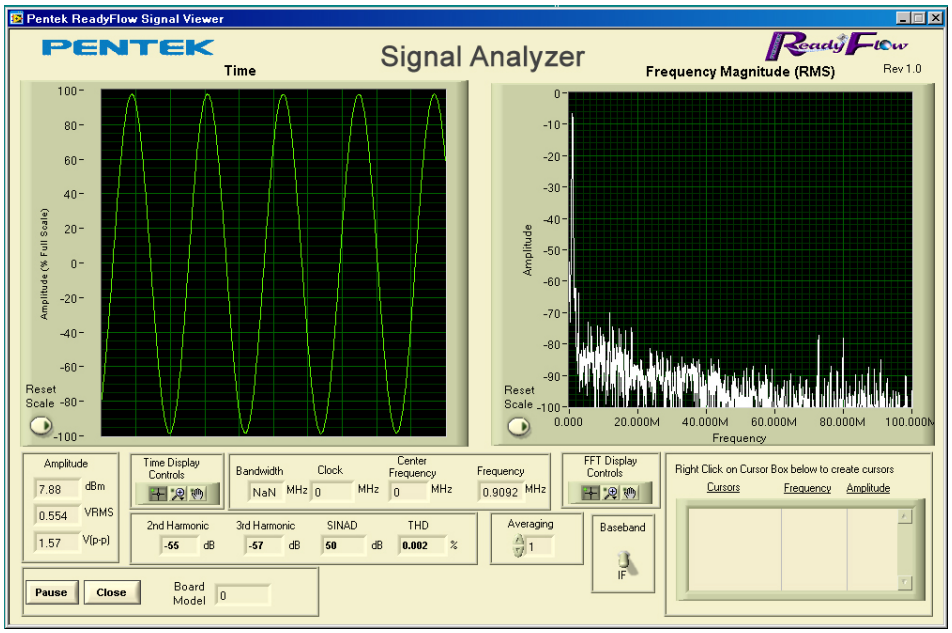
Model 4994A

Pentek ReadyFlow - Board Support Package for Linux™



Signal Analyzer*

When used with the Command Line Interface, the Signal Analyzer allows users to immediately start acquiring and displaying A/D data. A full-featured analysis tool, the Signal Analyzer displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals

Example, Model 71620

As an example of XMC module support, the BSP for the Cobalt® Model 71620 Transceiver with three 200 MHz A/Ds, DUC (Digital Upconverter), and two 800 MHz D/As includes data structures and routines to support the following:

- PCIe Bus interface and DMA controller
- Board control registers
- Timing bus control and clock selection
- Triggering, gate enable and polarity
- Data input device management for the 200 MHz A/D
- Data output device management for the DUC and the 800 MHz D/A
- Built-in A/D Data Acquisition IP Modules
- Built-in D/A Waveform Playback IP Modules
- Built-in test waveform generator
- Interrupt generation and handling
- FPGA configuration
- Test modes and hardware revision codes
- Hardware voltage and temperature monitor

Ordering Information

Model Description

4994A ReadyFlow - Board Support Package for Linux

Signal Analyzer and Command Line Interface supported on Cobalt series XMC, PCIe, VPX, and cPCI boards

* The signal viewer can only be run on an Intel PC running 32-bit Linux.

PowerPC Linux and Intel 64-bit Linux users have to run the viewer remotely on an Intel 32-bit Linux PC or on a 32- or 64-bit Windows PC.

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Pentek ReadyFlow - Board Support Package for Windows®

General Information

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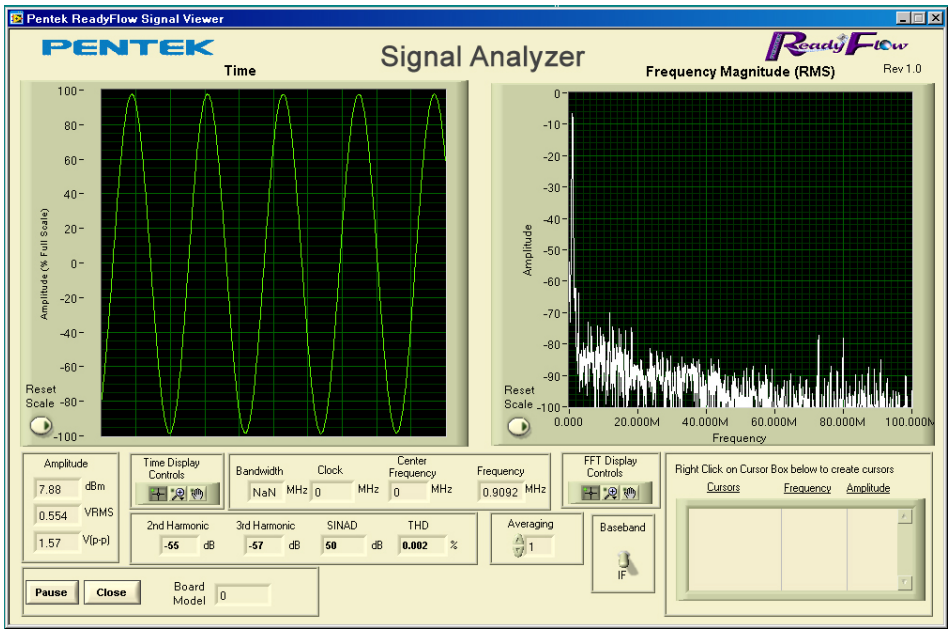
Model 4995A

Pentek ReadyFlow - Board Support Package for Windows®



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- Built-in D/A Waveform Playback IP Modules
- Built-in test waveform generator
- Interrupt generation and handling
- FPGA configuration
- Test modes and hardware revision codes
- Hardware voltage and temperature monitor

Ordering Information

Model	Description
4995A	ReadyFlow - Board Support Package for Windows

Signal Analyzer and Command Line Interface supported on Cobalt series XMC, PCIe, VPX, and cPCI boards

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Models 4996/4996A

Pentek VxWorks BSPs and Hardware Drivers

WIND RIVER PARTNER

Ordering Information

Model	Description
4996/4996A	Pentek VxWorks BSPs and Hardware Drivers

The Models 4996/4996A **VxWorks BSPs** provide software developers with a complete library of hardware initialization, control and application functions for Pentek PowerPC®/Power Architecture® processor baseboards, VME/VXS, PMC/XMC, VIM, and cPCI boards and modules. Used in conjunction with Wind River's **Workbench**® software development environment, they speed application development by providing a high-level API for accessing all of the processor board's memory and communication resources, and control of the board's I/O interfaces and I/O modules.

Processor specific functions found in the baseboard BSPs include: cache, DMA, SDRAM, interrupt, serial port, and timer control. Some general board functions include: reading and writing to mezzanine board FIFOs, VME/VXS, PMC/XMC, cPCI, and VIM I/O control, interprocessor communication, programming DMA reads and writes, programming interrupts, using mailboxes, managing RS-232 and ethernet interfaces, and control of optional Fibre Channel interfaces.

The VxWorks BSPs are designed to reduce development time not only during the initial stages of software development, but any time new I/O hardware is added to the system. **Hardware Drivers**, each designed to control the specific hardware features of the I/O interface being used, are built with a consistent style and function naming convention. Similar parameters on different I/O modules have similar driver calls, thereby allowing immediate familiarity with new I/O hardware as it's added. This can greatly shorten the application development learning curve when a system is modified or expanded.

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Wind River Workbench / VxWorks for PowerPC

Ordering Information

Contact Wind River Systems at:
www.windriver.com

Wind River's **Workbench** development platform has dramatically improved embedded developers' "time-to-productivity". A component of Workbench, Workbench Tools, comprises a comprehensive suite of core and optional cross-development tools and utilities. The other integrated components of Workbench consist of the VxWorks run-time system, a high-performance scalable real-time operating system that executes on the target processor and a full range of communications options for the target connection to the host. Workbench Tools provides a highly visual and automated environment that accelerates the development of even the most complex VxWorks-based applications.

At the heart of the VxWorks run-time system is the highly efficient Wind microkernel which supports a full range of real-time features. These include fast multitasking, interrupt support, and both preemptive and round-robin scheduling. The microkernel design minimizes system overhead and enables fast, deterministic response to external events.

SystemFlow® Recording Software

Features

- Complete turnkey recording and/or playback system software
- Software API for controlling data acquisition and recorder functions
- Graphical user interface
- Windows or Linux host
- One-year support included

General Information

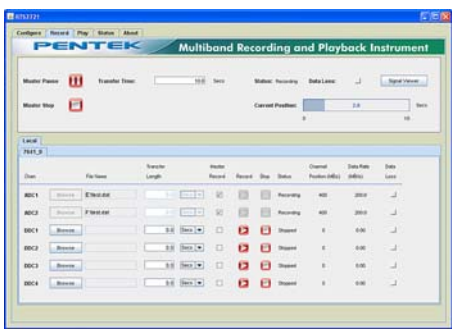
The Pentek SystemFlow Recording Software provides a rich set of function libraries and tools for controlling and building Pentek's real-time recording and data acquisition systems. These libraries ensure a consistent look and feel for developers across system families.

SystemFlow software allows developers to configure and customize system interfaces and behavior. It includes API functions not only for the real-time data acquisition and playback functions, but also for the user-control software running on the host PC including the GUI. These API functions allow developers to either modify the sample code to meet their needs or use it as a reference for custom software development.

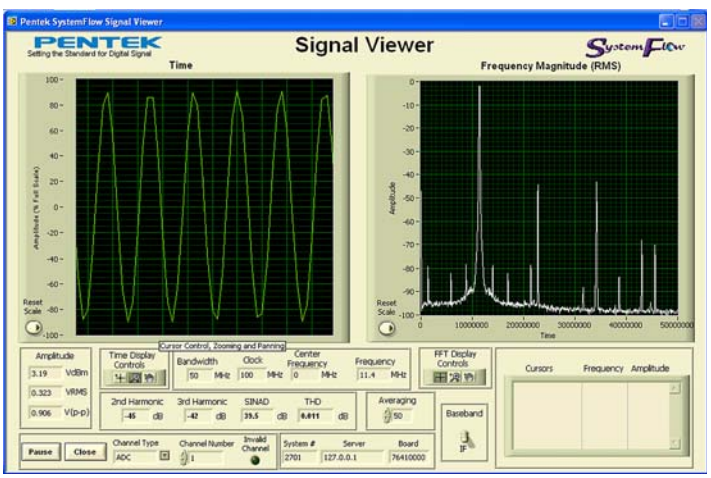
API Library Components

SystemFlow is based on a flexible client/server architecture. The host client application runs on a Windows or Linux platform and communicates with the server target application via a standard socket connection. In this way, server real-time recording and/or playback operations can be controlled from a local or remote host client.

All servers use PC hardware running under Windows. The server application includes scheduling, task management, full control of data from Pentek software radio hardware, and drivers for communication with the hard disk arrays.



Recorder Interface



Signal Viewer

SystemFlow Recorder Interface

The SystemFlow GUI provides the user with a control interface for recording data. It includes Configuration, Record, Playback and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperature and voltage levels. The signal viewer, integrated into the recording GUI, allows the user to monitor real-time signals or recorded signals on disk.

Hardware Configuration Interface

The SystemFlow configuration screens provide a simple and intuitive means for setting up the system parameters. The DDC configuration screen shown here, provides entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

Hardware Configuration Interface

SystemFlow Signal Viewer

The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.

More information on pentek.com

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Model 4986

Verari Systems Software VSI/Pro for PowerPC

The VSIPL (Vector, Signal and Image Processing Library) standard consists of definitions of over 500 scientific and engineering functions. It supports portable, high performance applications programming.

The standard is based upon existing libraries that have evolved and matured over decades of computing. These include functions for linear algebra, signal processing (FFTs, windowing, filtering and convolution routines), image processing, scalar functionality, and vector and matrix view functionalities (scalar, unary, binary and ternary operations).

The Verari Systems Software **VSI/Pro** is an implementation of VSIPL functions optimized specifically for the PowerPC and AltiVec architectures and is designed to be fully compliant with the emerging VSIPL standard.

As a commercial implementation, VSI/Pro is the immediate step between the VSIPL standard and your own specialized software application. The library is compatible with Wind River's VxWorks real-time operating system and supports the ANSI C and C++ languages.

Ordering Information

Model	Description
4986	Verari Systems Software VSI/Pro

Customer Information

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Carefully package the product in its original antistatic material, if it is still available, and ship it to us: prepaid (if within the US) or free domicile DDP (if outside the US). Show the RMA number on the outside of the package and include a written description of the malfunction.

When the work is completed, we will return the product to you free of charge, along with a statement of work done, if under warranty. Out-of-warranty work will be charged on a material and service time basis, and we will be happy to quote you a cost estimate for the repair and return shipping before proceeding.

Service phone: (201) 818-5900 • fax: (201) 818-5697 • email: **info@pentek.com**

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