Putting FPGAs to Work in Software Radio Systems

Sixth Edition

Technology

FPGA Resources

Products

Applications

Links

by

Rodger H. Hosking
Vice-President & Cofounder of Pentek, Inc.

Pentek, Inc.
One Park Way, Upper Saddle River, New Jersey 07458
Tel: (201) 818-5900 • Fax: (201) 818-5904
Email: info@pentek.com • http://www.pentek.com
Preface

FPGAs have become an increasingly important resource for software radio systems. Programmable logic technology now offers significant advantages for implementing software radio functions such as DDCs (Digital Downconverters). Over the past few years, the functions associated with DDCs have seen a shift from being delivered in ASICs (Application-Specific ICs) to operating as IP (Intellectual Property) in FPGAs.

For many applications, this implementation shift brings advantages that include design flexibility, higher precision processing, higher channel density, lower power, and lower cost per channel. With the advent of each new, higher-performance FPGA family, these benefits continue to increase.

This handbook introduces the basics of FPGA technology and its relationship to SDR (Software Defined Radio) systems. A review of Pentek’s GateFlow FPGA Design Resources is followed by a discussion of features and benefits of FPGA-based DDCs. Pentek SDR products that utilize FPGA technology and applications based on such products are also presented.

For a more in-depth discussion of SDR systems, the reader is referred to Pentek’s Software Defined Radio Handbook.

For more information on complementary subjects, the reader is referred to these Pentek Handbooks:
- Critical Techniques for High-Speed A/D Converters in Real-Time Systems
- High-Speed Switched Serial Fabrics Improve System Design
- High-Speed, Real-Time Recording Systems
We begin our discussion with the basic elements of a software radio receiver system.

The front end usually contains an analog RF amplifier and often an analog RF translator. This translates the high frequency RF signals down to a frequency that an A/D converter can handle. This is usually below 200 MHz and is often an IF output.

The A/D output feeds the DDC (Digital Down-converter) stage, which is typically contained in a monolithic chip which forms the heart of a software radio system.

Notice, that after the signal is digitized by the A/D converter, all further operations are performed by digital signal processing hardware.

Here we’ve ranked some of the popular signal processing tasks associated with SDR systems on a two axis graph, with compute Processing Intensity on the vertical axis and Flexibility on the horizontal axis.

What we mean by process intensity is the degree of highly-repetitive and rather primitive operations. At the upper left are dedicated functions like A/D converters and DDCs that require specialized hardware structures to complete the operations in real time. ASICs are usually chosen for these functions.

Flexibility pertains to the uniqueness or variability of the processing and how likely the function may have to be changed or customized for any specific application. At the lower right are tasks like analysis and decision-making which are highly variable and often subjective.

Programmable general purpose processors or DSPs are usually chosen for these tasks since these tasks can be easily changed by software.

Now let’s temporarily step away from the software radio tasks and take a deeper look at programmable logic devices.
Early Roles for FPGAs

- Used primarily to replace discrete digital hardware circuitry for:
  - Control logic
  - glue logic
  - Registers and gates
  - State machines
  - Counters and dividers
- Devices were selected by hardware engineers
- Programmed functions were seldom changed after the design went into production

Figure 3

As true programmable gate functions became available in the 1970’s, they were used extensively by hardware engineers to replace control logic, registers, gates and state machines which otherwise would have required many discrete, dedicated ICs.

Often these programmable logic devices were one-time factory-programmed parts that were soldered down and never changed after the design went into production.

Legacy FPGA Design Methodologies

- Tools were oriented to hardware engineers
  - Schematic processors
  - Boolean processors
  - Gates, registers, counters, multipliers
- Successful designs required high-level hardware engineering skills for:
  - Critical paths and propagation delays
  - Pin assignment and pin locking
  - Signal loading and drive capabilities
  - Clock distribution
  - Input signal synchronization and skew analysis

Figure 4

These programmable logic devices were mostly the domain of hardware engineers and the software tools were tailored to meet their needs. You had tools for accepting boolean equations or even schematics to help generate the interconnect pattern for the growing number of gates.

Then, programmable logic vendors started offering predefined logic blocks for flip-flops, registers and counters, that gave the engineer a leg up on popular hardware functions.

Nevertheless, the hardware engineer was still intimately involved with testing and evaluating the design using the same skills he needed for testing discrete logic designs. He had to worry about propagation delays, loading, clocking and synchronizing—all tricky problems that usually had to be solved the hard way—with oscilloscopes or logic analyzers.
Putting FPGAs to Work in Software Radio Systems

**Technology**

**FPGAs: New Device Technology**

- 500+ MHz DSP Slices and Memory Structures
- Over 3500 dedicated on-chip hardware multipliers
- On-board GHz Serial Transceivers
- Partial Reconfigurability Maintains
- Operation During Changes
- Switched Fabric Interface Engines
- Over 690,000 Logic Cells
- Gigabit Ethernet media access controllers
- On-chip 405 PowerPC RISC micro-controller cores
- Memory densities approaching 85 million bits
- Reduced power with core voltages at 1 volt
- Silicon geometries to 28 nanometers
- High-density BGA and flip-chip packaging
- Over 1200 user I/O pins
- Configurable logic and I/O interface standards

_Figure 5_

**FPGAs: New Development Tools**

- **High Level Design Tools**
  - Block Diagram System Generators
  - Schematic Processors
  - High-level language compilers for VHDL & Verilog
  - Advanced simulation tools for modeling speed, propagation delays, skew and board layout
  - Faster compilers and simulators save time
  - Graphically-oriented debugging tools

- **IP (Intellectual Property) Cores**
  - FPGA vendors offer both free and licensed cores
  - FPGA vendors promote third party core vendors
  - Wide range of IP cores available

_Figure 6_

It’s virtually impossible to keep up to date on FPGA technology, since new advancements are being made every day.

The hottest features are processor cores inside the chip, computation clocks to 500 MHz and above, and lower core voltages to keep power and heat down.

Several years ago, dedicated hardware multipliers started appearing and now you’ll find literally thousands of them on-chip as part of the DSP initiative launched by virtually all FPGA vendors.

High memory densities coupled with very flexible memory structures meet a wide range of data flow strategies. Logic slices with the equivalent of over ten million gates result from silicon geometries shrinking below 0.1 micron.

BGA and flip-chip packages provide plenty of I/O pins to support on-board gigabit serial transceivers and other user-configurable system interfaces.

New announcements seem to be coming out every day from chip vendors like Xilinx and Altera in a never-ending game of outperforming the competition.

To support such powerful devices, new design tools are appearing that now open up FPGAs to both hardware and software engineers. Instead of just accepting logic equations and schematics, these new tools accept entire block diagrams as well as VHDL and Verilog definitions.

Choosing the best FPGA vendor often hinges heavily on the quality of the design tools available to support the parts.

Excellent simulation and modeling tools help to quickly analyze worst case propagation delays and suggest alternate routing strategies to minimize them within the part. This minimizes some of the tricky timing work for hardware engineers and can save one hours of tedious troubleshooting during design verification and production testing.

In the last few years, a new industry of third party IP (Intellectual Property) core vendors now offer thousands of application-specific algorithms. These are ready to drop into the FPGA design process to help beat the time-to-market crunch and to minimize risk.
FPGAs for SDR

- Parallel Processing
- Hardware Multipliers for DSP
  - FPGAs can now have over 500 hardware multipliers
- Flexible Memory Structures
  - Dual port RAM, FIFOs, shift registers, look up tables, etc.
- Parallel and Pipelined Data Flow
  - Systolic simultaneous data movement
- Flexible I/O
  - Supports a variety of devices, buses and interface standards
- High Speed
- Available IP cores optimized for special functions

Like ASICs, all the logic elements in FPGAs can execute in parallel. This includes the hardware multipliers, and you can now get over 500 of them on a single FPGA.

This is in sharp contrast to programmable DSPs, which normally have just a handful of multipliers that must be operated sequentially.

FPGA memory can now be configured with the design tool to implement just the right structure for tasks that include dual port RAM, FIFOs, shift registers and other popular memory types.

These memories can be distributed along the signal path or interspersed with the multipliers and math blocks, so that the whole signal processing task operates in parallel in a systolic pipelined fashion.

Again, this is dramatically different from sequential execution and data fetches from external memory as in a programmable DSP.

As we said, FPGAs now have specialized serial and parallel interfaces to match requirements for high-speed peripherals and buses.

As a result, FPGAs have significantly invaded the application task space as shown by the center bubble in the task diagram above.

They offer the advantages of parallel hardware to handle some of the high process intensity functions like DDCs and the benefit of programmability to accommodate some of the decoding and analysis functions of DSPs.

These advantages may come at the expense of increased power dissipation and increased product costs. However, these considerations are often secondary to the performance and capabilities of these remarkable devices.
### FPGA Resource Comparison

<table>
<thead>
<tr>
<th></th>
<th>Virtex-II Pro</th>
<th>Virtex-4</th>
<th>Virtex-5</th>
<th>Virtex-6</th>
<th>Virtex-7</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>VP50, VP70</td>
<td>FX, LX, SX</td>
<td>LXT, SXT</td>
<td>LXT, SXT</td>
<td>330T, 690T</td>
</tr>
<tr>
<td>Block RAM (kb)</td>
<td>4,176–5,904</td>
<td>4,176–6,768</td>
<td>4,752–8,784</td>
<td>9,504–36,304</td>
<td>27,000–52,920</td>
</tr>
<tr>
<td>DSP Hard IP</td>
<td>18x18 Multipliers</td>
<td>DSP48</td>
<td>DSP48E</td>
<td>DSP48E</td>
<td>DSP48E</td>
</tr>
<tr>
<td>DSP Slices</td>
<td>232–328</td>
<td>96–512</td>
<td>128–640</td>
<td>480–2,016</td>
<td>1,120–3,600</td>
</tr>
<tr>
<td>Serial Gbit Transceivers</td>
<td>–</td>
<td>0–20</td>
<td>12–16</td>
<td>20–48</td>
<td>20–48</td>
</tr>
<tr>
<td>PCI Express Support</td>
<td>–</td>
<td>–</td>
<td>–</td>
<td>Gen2x8</td>
<td>Gen2x8, Gen3x8</td>
</tr>
<tr>
<td>SelectIO</td>
<td>–</td>
<td>448–768</td>
<td>480–640</td>
<td>320–600</td>
<td>300–600</td>
</tr>
</tbody>
</table>

*Virtex-II Pro and Virtex-4 Slices actually require 2.25 Logic Cells; *Virtex-5, Virtex-6 and Virtex-7 Slices actually require 6.4 Logic Cells

The above chart compares the available resources in the five Xilinx FPGA families that are used in most of the Pentek products.

- Virtex-II Pro: VP50 and VP70
- Virtex-4: FX, LX and SX
- Virtex-5: LXT and SXT
- Virtex-6: LXT and SXT
- Virtex-7: 330T and 690T

The Virtex-II family includes hardware multipliers that support digital filters, averagers, demodulators and FFTs—a major benefit for software radio signal processing. The Virtex-II Pro family dramatically increased the number of hardware multipliers and also added embedded PowerPC microcontrollers.

The Virtex-4 family is offered as three subfamilies that dramatically boost clock speeds and reduce power dissipation over previous generations.

The Virtex-4 LX family delivers maximum logic and I/O pins while the SX family boasts of 512 DSP slices for maximum DSP performance. The FX family is a generous mix of all resources and is the only family to offer RocketIO, PowerPC cores, and the newly added gigabit Ethernet ports.

The Virtex-5 family LXT devices offer maximum logic resources, gigabit serial transceivers, and Ethernet media access controllers. The SXT devices push DSP capabilities with all of the same extras as the LXT.

The Virtex-5 devices offer lower power dissipation, faster clock speeds and enhanced logic slices. They also improve the clocking features to handle faster memory and gigabit interfaces. They support faster single-ended and differential parallel I/O buses to handle faster peripheral devices.

The Virtex-6 and Virtex-7 devices offer still higher density, more processing power, lower power consumption, and updated interface features to match the latest technology I/O requirements including PCI Express. Virtex-6 supports PCIe 2.0 and Virtex-7 supports PCIe 3.0.

The ample DSP slices are responsible for the majority of the processing power of the Virtex-6 and Virtex-7 families. Increases in operating speed from 500 MHz in V-4, to 550 MHz in V-5, to 600 MHz in V-6, to 900 MHz in V-7 and continuously increasing density allow more DSP slices to be included in the same-size package. As shown in the chart, Virtex-6 tops out at an impressive 2,016 DSP slices, while Virtex-7 tops out at an even more impressive 3,600 DSP slices.
GateFlow Design Resources

GateFlow is Pentek’s flagship collection of FPGA Design Resources. The GateFlow line is compatible with the Xilinx Virtex products and is available as two separate offerings:

If you want to add your own custom algorithms, we offer the GateFlow FPGA Design Kit.

We also offer popular high-performance signal-processing algorithms with the GateFlow factory-installed IP Cores. These algorithms are designed expressly for Xilinx FPGAs and Pentek hardware products.

Installed Cores are delivered to you preinstalled in your Pentek FPGA-based product of choice and are fully supported with Pentek ReadyFlow Board Support Packages.

Let’s start with the GateFlow FPGA Design Kit.

GateFlow FPGA Design Kit

- Allows FPGA design engineers to easily add functions to standard factory configuration
- Includes VHDL source code for all standard functions:
  - Control and status registers
  - A/D and Digital receiver interfaces
  - Mezzanine interfaces
  - Triggering, clocking, sync and gating functions
  - Data packing and formatting
  - Channel selection
  - A/D / Receiver multiplexing
  - Interrupt generation
  - Data tagging and channel ID
- User Block for inserting custom code

If you want to add your own algorithms to Pentek catalog products, we offer the GateFlow FPGA Design Kit that includes VHDL source code for all the standard factory functions.

VHDL is one of the most popular languages used in the FPGA design tools. The GateFlow Design Kit includes the VHDL source code for every software module we use to create these standard factory features of the product.

The standard factory configuration supports a wide range of operating modes, timing and sync functions, as well as several different data formatting options.

This includes control and status registers, peripheral interfaces, mezzanine interfaces, timing functions, data formatting, channel selection, interrupt support, and data tagging.

These are also fully supported with our ReadyFlow Board Support Package.
The GateFlow FPGA Design Kit allows the user to modify, replace and extend the standard factory-installed functions in the FPGA to incorporate special modes of operation, new control structures, and specialized signal-processing algorithms.

The Cobalt and Onyx architectures configure the FPGA with standard factory-supplied interfaces including memory controllers, DMA engines, A/D and D/A interfaces, timing and synchronization structures, triggering and gating logic, time stamping and header tagging, data formatting engines, and the PCIe interface. These resources are connected to the User Application Container using well-defined ports that present easy-to-use data and control signals, effectively abstracting the lower level details of the hardware.

Shown here is the FPGA block diagram of a typical Cobalt or Onyx module. The User Application Container holds a collection of different factory-installed IP modules connected to the various interfaces through the standard ports surrounding the container. The specific IP modules for each product are described in further detail in the datasheet of that product.

The GateFlow Design Kit provides a complete Xilinx ISE Foundation Tool project folder containing all the files necessary for the FPGA developer to recompile the entire project with or without any required changes. VHDL source code for each IP module provides excellent examples of how the IP modules work, how they might be modified, and how they might be replaced with custom IP to implement a specific function.
The **GateFlow** FPGA Design Kit is intended for the programming of predefined user blocks located in the data flow path specifically reserved for custom applications. These predefined blocks protect users from inadvertently altering base functionality.

Pentek recommends user programming be limited to the predefined user blocks to maintain base functionality. However, for more complex requirements, sufficient information is supplied in the kit for the user to modify, add to, or replace default board functions if necessary. Default configuration files are included with the Design Kit should it be necessary to restore standard factory configuration.

Shown above is the block diagram of a typical software radio module. The diagram includes the FPGA and external hardware devices connected to it.

The blocks inside the FPGA are VHDL code modules that handle the standard factory functions and interfaces. The User Block is a VHDL module that sits in the data path with pin definitions for input, output, status, control and clocks.

In the standard Design Kit product, the User Block is configured as a straight wire between the input and output ports. By creating a custom algorithm inside the block that conforms to the pin definition, the user will have a low-risk experience in recompiling and installing the custom code. Since Pentek provides source code for all the modules, changes outside the user block can also be made by the user.
Pentek is an AllianceCore Member, a third party program sponsored by Xilinx for companies that specialize in specific areas of expertise in developing FPGA algorithms for niche application areas. These include image processing, communications, telecom, telemetry, signal intelligence, wireless communications, wireless networking, and many other disciplines.

Pentek offers popular high-performance signal processing algorithms installed in Pentek products. These algorithms are designed expressly for Xilinx FPGAs and Pentek hardware products. The cores take full advantage of the numerous hardware multipliers to achieve highly-parallel processing structures that can dramatically outperform programmable RISC and DSP processors.

Installed Cores are optimized for efficient FPGA resource utilization, execution and throughput speed. They are delivered to you preinstalled in your Pentek FPGA-based product of choice and are fully tested and supported with the Pentek ReadyFlow Board Support Packages. Purchasing these popular factory-installed cores saves you the time and costs of acquiring FPGA tools and developing custom FPGA code.
Over the past few years, the functions associated with DDCs have seen a shift from being delivered in ASICs (Application-Specific ICs) to operating as IP (Intellectual Property) in FPGAs.

For many applications, this implementation shift brings advantages that include: design flexibility, higher precision processing, higher channel density, lower power, and lower cost per channel. With the advent of each new higher performance FPGA family during the past few years, these benefits continue to increase.

To understand how FPGAs play a key role in implementing DDCs that perform the function of a receiver, it’s important to break the DDC down into its individual functional blocks. The block diagram shows a classic DDC. Regardless of whether it’s implemented in an ASIC or an FPGA, this is the common architecture of the DDC function.

The first stage of the DDC uses a complex digital mixer to translate the frequency of interest down to baseband. It uses a pair of multipliers and a DDS (Direct Digital Synthesizer) as the NCO (Numerically Controlled Oscillator). This function enables the user to tune the receiver to the desired frequency of interest. The second stage of the DDC reduces the sampling frequency of the signal to match the desired output bandwidth. It uses a CIC (Cascaded Integrator Comb) filter to decimate the data.

A second CIC filter provides a coarse gain adjustment stage. The signal is then passed to a pair of additional polyphase filters. First a CFIR (Compensation Finite Impulse Response) filter then to a PFIR (Programmable Finite Impulse Response) filter. This filter pair provides additional decimation and final signal shaping prior to the rounding stage and final output.

When we get past all the acronyms, we realize that most of the individual function blocks of the DDC are implemented using multipliers. It thus becomes apparent how the DDC might map into current FPGA families. Most new FPGAs include a wealth of DSP function blocks which are primarily multipliers. The general purpose logic resource and on-chip memory of FPGAs also match the requirements of the DDC for implementing the required FIR filters and filter coefficient tables.

As part of their IP library series, Xilinx provides a free DDC core. The core serves as a good general reference design, following the classic DDC architecture shown here. While this core can be used as a building block for general purpose DDCs, the real advantages of an IP-based implementation can be best seen in optimized custom cores that are designed to match the requirements of a specific application.
Putting FPGAs to Work in Software Radio Systems

FPGA Resources

IP Enables Software Radio Products

<table>
<thead>
<tr>
<th>DDC Implementation</th>
<th>Number of Channels</th>
<th>Decimation Range</th>
<th>Input Rate (MHz)</th>
<th>SFDR (dBFS)</th>
<th>Decimation Steps</th>
<th>Area per Channel (mm²)¹</th>
<th>Power per Channel (W)²</th>
<th>Cost per Channel ($)³</th>
</tr>
</thead>
<tbody>
<tr>
<td>TI GC4016 ASIC</td>
<td>4</td>
<td>32–16,384</td>
<td>160</td>
<td>115</td>
<td>1</td>
<td>72.3</td>
<td>0.25</td>
<td>41</td>
</tr>
<tr>
<td>Pentek 7141-420</td>
<td>2</td>
<td>2–64</td>
<td>110</td>
<td>118</td>
<td>Binary</td>
<td>612.5</td>
<td>2.5</td>
<td>204</td>
</tr>
<tr>
<td>Pentek 7141-430</td>
<td>256</td>
<td>1,024–9,984</td>
<td>110</td>
<td>110</td>
<td>256</td>
<td>4.7</td>
<td>0.01</td>
<td>2</td>
</tr>
<tr>
<td>Pentek 7142-428</td>
<td>4</td>
<td>2–65,536</td>
<td>125</td>
<td>108</td>
<td>1</td>
<td>206.2</td>
<td>2.0</td>
<td>102</td>
</tr>
<tr>
<td>Pentek 7151</td>
<td>256</td>
<td>128–1,024</td>
<td>200</td>
<td>105</td>
<td>64</td>
<td>4.7</td>
<td>0.04</td>
<td>6</td>
</tr>
<tr>
<td>Pentek 7152</td>
<td>32</td>
<td>16–8,192</td>
<td>200</td>
<td>105</td>
<td>8</td>
<td>38.3</td>
<td>0.25</td>
<td>44</td>
</tr>
<tr>
<td>Pentek 7153</td>
<td>4</td>
<td>2–256</td>
<td>200</td>
<td>120</td>
<td>1</td>
<td>206.2</td>
<td>1.25</td>
<td>29</td>
</tr>
<tr>
<td>Pentek 7153</td>
<td>2</td>
<td>2–65,536</td>
<td>200</td>
<td>120</td>
<td>1</td>
<td>612.5</td>
<td>2.5</td>
<td>57</td>
</tr>
</tbody>
</table>

Note ¹: Area per Channel = IC area ÷ number of channels.

Note ²: GC4016 Power per Channel = Total IC power ÷ number of channels, IP Core Power per Channel = (FPGA power with IP core – FPGA power without IP core) ÷ number of channels.

Note ³: GC4016 Cost per Channel = cost of IC ÷ number of channels; IP core Cost per Channel = cost of FPGA resources used ÷ number of channels.

Figure 16

Pentek offers a series of high-performance IP-based DDCs, available preinstalled in software radio modules. Each is optimized to match a specific range of application requirements.

These cores range from the high-channel count/narrow bandwidth of the 430 Core installed in the Model 7141, to the wider bandwidths and excellent SFDR (Spurious Free Dynamic Range) of the core installed in the Model 7153.

The above table lists some of the DDC cores available from Pentek as software radio modules. For each core, pertinent specifications are listed. These products are available in industry standard PMC/XMC modules as well as 3U and 6U CompactPCI, PCI, PCI Express and OpenVPX form factors. In addition to the IP-based solutions, a popular ASIC-based DDC solution from Texas Instruments, the GC4016, is included as a reference.

When compared on a size/power/cost per channel basis, it becomes apparent that narrowband, high channel-count DDC cores can be very efficiently implemented in FPGAs. Implementation of wideband DDCs consumes many more FPGA DSP and logic resources. As a result, the number of channels that can be fit into a single FPGA is limited. Even with less cost-effective wideband DDCs, the custom IP approach can sometimes provide the only viable solution when a specific performance characteristic is required. The improved SFDR of the Pentek 420 core is an example of such a requirement.
An additional benefit of IP based solutions is the flexible nature of their implementation. The Models 7141-420 and 7141-430 are created by using the same hardware base with different installed IP cores. Similarly, the Models 7151, 7152 and 7153 are all based on the same 4-channel, 200 MHz, 16-bit A/D PMC/XMC with different FPGA IP cores. All share the same software base allowing migration between different applications to be accomplished with minimum software porting.

Additionally, some applications like JTRS (Joint Tactical Radio System), need to operate across a wide spectrum to handle the diverse signal types. Such applications can benefit greatly by IP based solutions. This Figure, shows the six optimized Pentek cores across a range of applications and the number of channels and bandwidth they typically require.

Again, this wide range of applications can be satisfied by using a small set of hardware with different, optimized IP cores. This is one of the fundamental concepts of SDR (Software Defined Radio), and it's difficult, if not impossible, to achieve with ASIC-based solutions.
Let’s now take a look at a complete receiver system. One common application is GSM 2G, a high channel count, low bandwidth system. An E-GMS receiver requires 174 channels spaced 200 kHz apart. Just three or four years ago, a viable solution would have used the TI/Graychip 4-channel GC4016 ASIC-based DDCs. A common board form factor for these types of application is PMC, such as the Pentek Model 7131. One PMC can house two 100MHz A/Ds and four GC4016s and all of the required interface and support circuitry. For a 174-channel system this would require 11 Model 7131’s.

By comparison, an IP DDC with 174 channels and similar performance to the 4016 can fit in a single Virtex-5 XC5VSX95T FPGA that can be housed in a single PMC, along with four channels of 200MHz A/Ds and all support circuitry such as the Pentek Model 7151. A visual comparison of these two solutions is shown in the above figure.

FPGAs continue to offer new possibilities and performance when addressing processing tasks like digital downconversion. With each new generation of higher performance FPGAs, processing precision continues to increase. This enables IP-based DDCs to outperform their ASIC-based cousins with specifications like better SFDR.

As shown in this figure, it’s easy to understand how packing many channels of DDCs into one or two FPGAs can reduce the board count, power requirements and cost over a solution that requires 30 or 40 individual ASIC DDC chips. Additionally, FPGA solutions are extremely flexible since they can support vastly different signals with the simple loading of a different IP core while using the same hardware platform.

FPGA solutions are not a perfect match for all requirements. They show the greatest advantages in systems with high channel densities and, typically, narrower bandwidths. In systems with just one or two channels and bandwidths in the range of 100 MHz or greater, the higher cost of the FPGAs needed can quickly exceed the cost of designing the system with a single multichannel DDC ASIC. Again, while cost, size and power are important factors in designing a receiver system, ultimately the technical requirements may require the choice of an ASIC or FPGA solution.
The Pentek family of board-level software radio products is the most comprehensive in the industry. Most of these products are available in several formats to satisfy a wide range of requirements.

In addition to their commercial versions, many software radio products are available in ruggedized and conduction-cooled versions.

All of the software radio products include input A/D converters. Some of these products are software radio receivers in that they include only DDCs. Others are software radio transceivers and they include DDCs as well as DUCs with output D/A converters. These come with independent input and output clocks.

All Pentek software radio products include multiboard synchronization that facilitates the design of multichannel systems with synchronous clocking, gating and triggering.

Pentek's comprehensive software support includes the ReadyFlow Board Support Package, the GateFlow FPGA Design Kit and high-performance factory-installed IP cores that expand the features and range of many Pentek software radio products. In addition, Pentek software radio recording systems are supported with SystemFlow® recording software that features a graphical user interface.

A complete listing of these products with active links to their datasheets on Pentek’s website is included at the end of this handbook.
The Model 7131, a 16-Channel Multiband Receiver, is a PMC module. The 7131 PMC may be attached to a wide range of industry processor platforms equipped with PMC sites.

Two 14-bit 105 MHz A/D Converters accept transformer-coupled RF inputs through two front panel SMA connectors. Both inputs are connected to four TI/GC4016 quad DDC chips, so that all 16 DDC channels can independently select either A/D.

Four parallel outputs from the four DDCs deliver data into the Virtex-II FPGA which can be either the XC2V1000 or XC2V3000. The outputs of the two A/D converters are also connected directly to the FPGA to support the DDC bypass path to the PCI bus and for direct processing of the wideband A/D signals by the FPGA.

The unit supports the channel combining mode of the 4016s such that two or four individual 2.5 MHz channels can be combined for output bandwidths of 5 MHz or 10 MHz, respectively.

The sampling clock can be sourced from an internal 100 MHz crystal oscillator or from an external clock supplied through an SMA connector or the LVDS clock/sync bus on the front panel. The LVDS bus allows multiple modules to be synchronized with the same sample clock, gating, triggering and frequency switching signals. Up to 80 modules can be synchronized with the Model 9190 Clock and Sync Generator. Custom interfaces can be implemented by using the 64 user-defined FPGA I/O pins on the P4 connector.

Versions of the 7131 are also available as a PCI board (Model 7631A), 6U cPCI (Models 7231 and 7231D dual density), 3U cPCI (Model 7331) and 3U VPX (Model 5331). All these products have similar features.
The Model 7141 PMC/XMC module combines both receive and transmit capabilities with a high-performance Virtex II-Pro FPGA and supports the VITA 42 XMC standard with optional switched fabric interfaces for high-speed I/O.

The front end of the module accepts two RF inputs and transformer-couples them into two 14-bit A/D converters running at 125 MHz. The digitized output signals pass to a Virtex-II Pro FPGA for signal processing or routing to other module resources.

These resources include a quad digital downconverter, a digital upconverter with dual D/A converters, 512 MB DDR SDRAM delay memory and the PCI bus. The FPGA also serves as a control and status engine with data and programming interfaces to each of the on-board resources. Factory-installed FPGA functions include data multiplexing, channel selection, data packing, gating, triggering, and SDRAM memory control.

In addition to acting as a simple transceiver, the module can perform user-defined DSP functions on the baseband signals, developed using Pentek’s GateFlow and ReadyFlow development tools.

The module includes a TI/GC4016 quad digital downconverter along with a TI DAC5686 digital upconverter with dual D/A converters.

Each channel in the downconverter can be set with an independent tuning frequency and bandwidth. The upconverter translates a real or complex baseband signal to any IF center frequency from DC to 160 MHz and can deliver real or complex (I + Q) analog outputs through its two 16-bit D/A converters. The digital upconverter can be bypassed for two interpolated D/A outputs with sampling rates to 500 MHz.

Versions of the 7141 are also available as a PCIe full-length board (Models 7741 and 7741D dual density), PCIe half-length board (Model 7841), 3U VPX board (Model 5341), PCI board (Model 7641), 6U cPCI (Models 7241 and 7241D dual density), and 3U cPCI (Model 7341).

Model 7141-703 is a conduction-cooled version.
The Pentek IP Core 420 includes a dual high-performance wideband DDC and an interpolation filter. Factory-installed in the Model 7141 FPGA, they extend the range of both the GC4016 ASIC DDC and the DAC5686 DUC.

Each of the core 420 DDCs translates any frequency band within the input bandwidth range down to zero frequency. A complex FIR low pass filter removes any out-of-band frequency components. An output decimator and formatter deliver either complex or real data. An input gain block scales both I and Q data streams by a 16-bit gain term.

The mixer utilizes four 18x18-bit multipliers to handle the complex inputs from the NCO and the complex data input samples. The FIR filter is capable of storing and utilizing up to four independent sets of 18-bit coefficients for each decimation value. These coefficients are user-programmable by using RAM structures within the FPGA.

The decimation settings of 2, 4, 8, 16, 32, and 64 provide output bandwidths from 40 MHz down to 1.25 MHz for an A/D sampling of 100 MHz. A multiplexer allows data to be sourced from either the A/Ds or the GC4016, extending the cascaded decimation range to 1,048,576.

The interpolation filter included in the 420 Core, expands the interpolation factor from 2 to 32,768 programmable in steps of 2, and relieves the host processor from performing upsampling tasks. Including the DUC, the maximum interpolation factor is 32,768 which is comparable to the maximum decimation of the GC4016 narrowband DDC.

Versions of the 7141-420 are also available as a 3U VPX board (Model 5341-420), PCIe full-length board (Models 7741-420 and 7741D-420 dual density), PCIe half-length board (Model 7841-420), PCI board (Model 7641-420), 6U cPCI (Models 7241-420 and 7241D-420 dual density), or 3U cPCI (Model 7341-420). Model 7141-703-420 is a conduction-cooled version.
For applications that require many channels of narrowband downconverters, Pentek offers the GateFlow IP Core 430 256-channel digital downconverter bank. Factory installed in the Model 7141 FPGA, Core 430 creates a flexible, very high-channel count receiver system in a small footprint.

Unlike classic channelizer methods, the Pentek 430 core allows for completely independent programmable tuning of each individual channel with 32-bit resolution as well as filter characteristics comparable to many conventional ASIC DDCs.

Added flexibility comes from programmable global decimation settings ranging from 1024 to 8192 in steps of 256, and 18-bit user programmable FIR decimating filter coefficients for the DDCs. Default DDC filter coefficient sets are included with the core for all possible decimation settings.

Core 430 utilizes a unique method of channelization. It differs from others in that the channel center frequencies need not be at fixed intervals, and are independently programmable to any value.

Core 430 DDC comes factory installed in the Model 7141-430. A multiplexer allows data to be sourced from either A/D. At the output, a multiplexer allows for routing either the output of the GC4016 or the 430 DDC to the PCI Bus.

In addition to the DDC outputs, data from both A/D channels are presented to the PCI Bus at a rate equal to the A/D clock rate divided by any integer value between 1 and 4096. A TI DAC5686 digital upconverter and dual D/A accepts baseband real or complex data streams from the PCI Bus with signal bandwidths up to 50 MHz.

Versions of the 7141-430 are also available as a PCIe full-length board (Models 7741-430 and 7741D-430 dual density), PCIe half-length board (Model 7841-430), 3U VPX board (Model 5341-430), PCI board (Model 7641-430), 6U cPCI (Models 7241-430 and 7241D-430 dual density), or 3U cPCI (Model 7341-430). Model 7141-703-430 is a conduction-cooled version.
The Model 7142 is a Multichannel PMC/XMC module. It includes four 125 MHz 14-bit A/D converters and one upconverter with a 500 MHz 16-bit D/A converter to support wideband receive and transmit communication channels.

Two Xilinx Virtex-4 FPGAs are included: an XC4VSX55 or LX100 and an XC4VFX60 or FX100. The first FPGA is used for control and signal processing functions, while the second one is used for implementing board interface functions including the XMC interface.

It also features 768 MB of SDRAM for implementing up to 2.0 sec of transient capture or digital delay memory for signal intelligence tracking applications at 125 MHz.

A 16 MB flash memory supports the boot code for the two on-board IBM 405 PowerPC microcontroller cores within the FPGA.

A 9-channel DMA controller and 64 bit / 66 MHz PCI interface assures efficient transfers to and from the module.

A high-performance 160 MHz IP core wideband digital downconverter may be factory-installed in the first FPGA.

Two 4X switched serial ports, implemented with the Xilinx Rocket I/O interfaces, connect the second FPGA to the XMC connector with two 2.5 GB/sec data links to the carrier board.

A dual bus system timing generator allows separate clocks, gates and synchronization signals for the A/D and D/A converters. It also supports large, multichannel applications where the relative phases must be preserved.

Versions of the 7142 are also available as a PCIe full-length board (Models 7742 and 7742D dual density), PCIe half-length board (Model 7842), 3U VPX (Model 5342), PCI board (Model 7642), 6U cPCI (Models 7242 and 7242D dual density), and 3U cPCI (Model 7342).
Putting FPGAs to Work in Software Radio Systems

The Pentek IP Core 428 includes four high-performance multiband DDCs and an interpolation filter. Factory-installed in the Model 7142 FPGA, they add DDCs to the Model 7142 and extend the range of its DAC5686 DUC.

The Core 428 downconverter translates any frequency band within the input bandwidth range down to zero frequency. The DDCs consist of two cascaded decimating FIR filters. The decimation of each DDC can be set independently. After each filter stage is a post filter gain stage. This gain may be used to amplify small signals after out-of-band signals have been filtered out.

The NCO provides over 108 dB spurious-free dynamic range (SFDR). The FIR filter is capable of storing and utilizing two independent sets of 18-bit coefficients. These coefficients are user-programmable by using RAM structures within the FPGA. NCO tuning frequency, decimation and filter coefficients can be changed dynamically.

Four identical Core 428 DDCs are factory installed in the 7142-428 FPGA. An input multiplexer allows any DDC to independently select any of the four A/D sources. The overall decimation range from 2 to 65,536, programmable in steps of 1, provides output bandwidths from 50 MHz down to 1.52 kHz for an A/D sampling rate of 125 MHz and assuming an 80% filter.

The Core 428 interpolation filter increases the sampling rate of real or complex baseband signals by a factor of 16 to 2048, programmable in steps of 4, and relieves the host processor from performing upsampling tasks. The interpolation filter can be used in series with the DUC’s built-in interpolation, for a maximum interpolation of 32,768.

Versions of the 7142-428 are also available as a PCIe full-length board (Models 7742-428 and 7742D-428 dual density), PCIe half-length board (Model 7842-428), PCI board (Model 7642-428), 6U cPCI (Models 7242-428 and 7242D-428 dual density), 3U cPCI (Model 7342-428), and 3U VPX (Model 5342-428).
The Model 7151 PMC module is a 4-channel high-speed digitizer with a factory-installed 256-channel DDC core. The front end of the module accepts four RF inputs and transformer-couples them into four 16-bit A/D converters running at 200 MHz. The digitized output signals pass to a Virtex-5 FPGA for routing, formatting and DDC signal processing.

The Model 7151 employs an advanced FPGA-based digital downconverter engine consisting of four identical 64-channel DDC banks. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC bank. Each of the 256 DDCs has an independent 32-bit tuning frequency setting.

All of the 64 channels within a bank share a common decimation setting that can range from 128 to 1024, programmable in steps of 64. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 156.25 kHz to 1.25 MHz. Each 64-channel bank can have its own unique decimation setting supporting as many as four different output bandwidths for the board.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8* f_s/N$, where $N$ is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples. Any number of channels can be enabled within each bank, selectable from 0 to 64. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within the bank.

Versions of the 7151 are also available as a PCIe full-length board (Models 7751 and 7751D dual density), PCIe half-length board (Model 7851), PCI board (Model 7651), 6U cPCI (Models 7251 and 7251D dual density), 3U cPCI (Model 7351), and 3U VPX (Model 5351).
The Model 7152 PMC module is a 4-channel high-speed digitizer with a factory-installed 32-channel DDC core. The front end of the module accepts four RF inputs and transformer-couples them into four 16-bit A/D converters running at 200 MHz. The digitized output signals pass to a Virtex-5 FPGA for routing, formatting and DDC signal processing.

The Model 7152 employs an advanced FPGA-based digital downconverter engine consisting of four identical 8-channel DDC banks. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC bank. Each of the 32 DDCs has an independent 32-bit tuning frequency setting.

All of the 8 channels within a bank share a common decimation setting that can range from 16 to 8192, programmable in steps of 8. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have its own unique decimation setting supporting as many as four different output bandwidths for the board.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8*fs/N, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples. Any number of channels can be enabled within each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within the bank. Gain and phase control, power meters and threshold detectors are included.

Versions of the 7152 are also available as a PCIe full-length board (Models 7752 and 7752D dual density), PCIe half-length board (Model 7852), PCI board (Model 7652), 6U cPCI (Models 7252 and 7252D dual density), 3U cPCI (Model 7352), and 3U VPX (Model 5352).
Model 7153 is a 4-channel, high-speed software radio module designed for processing baseband RF or IF signals. It features four 200 MHz 16-bit A/Ds supported by a high-performance 4-channel DDC (digital downconverter) installed core and a complete set of beamforming functions. With built-in multiboard synchronization and an Aurora gigabit serial interface, it provides everything needed for implementing multichannel beamforming systems.

The Model 7153 employs an advanced FPGA-based DDC engine consisting of four identical multiband banks. Four independently controllable input multiplexers select one of the four A/Ds as the input source for each DDC bank. Each of the 4 DDCs has an independent 32-bit tuning frequency setting.

All four DDCs have a decimation setting that can range from 2 to 256, programmable independently in steps of 1. The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of 0.8*\( f_s/N \), where N is the decimation setting. The rejection of adjacent-band components within the 80% output band-width is better than 100 dB.

In addition to the DDCs, the 7153 features a complete beamforming subsystem. Each channel contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8 ksamples. The power meters present average power measurements for each channel in easy-to-read registers. Each channel also includes a threshold detector that sends an interrupt to the processor if the average power level of any DDC falls below or exceeds a programmable threshold.

Versions of the 7153 are also available as a PCIe full-length board (Models 7753 and 7753D dual density), PCIe half-length board (Model 7853), PCI board (Model 7653), 6U cPCI (Models 7253 and 7253D dual density), 3U cPCI (Model 7353), and 3U VPX (Model 5353).
Model 7156 is a dual high-speed data converter suitable for connection as the HF or IF input of a communications system. It features two 400 MHz 14-bit A/Ds, a DUC with two 800 MHz 16-bit D/As, and two Virtex-5 FPGAs. Model 7156 uses the popular PMC format and supports the VITA 42 XMC standard for switched fabric interfaces.

The Model 7156 architecture includes two Virtex-5 FPGAs. The first FPGA is used primarily for signal processing while the second one is dedicated to board interfaces. All of the board’s data and control paths are accessible by the FPGAs, enabling factory installed functions such as data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control.

Two independent 512 MB banks of DDR2 SDRAM are available to the signal processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. All memory banks can be easily accessed through the PCI-X interface.

A high-performance IP core wideband DDC may be factory-installed in the processing FPGA.

A 5-channel DMA controller and 64 bit/100 MHz PCI-X interface assures efficient transfers to and from the module.

Two 4X switched serial ports implemented with the Xilinx Rocket I/O interfaces, connect the FPGA to the XMC connector with two 2.5 GB/sec data links to the carrier board.

A dual bus system timing generator allows for sample clock synchronization to an external system reference. It also supports large, multichannel applications where the relative phases must be preserved.

Versions of the 7156 are also available as a PCIe full-length board (Models 7756 and 7756D dual density), PCIe half-length board (Model 7856), PCI board (Model 7656), 6U cPCI (Models 7256 and 7256D dual density), 3U cPCI (Model 7356), and 3U VPX (Model 5356). All these products have similar features.
Putting FPGAs to Work in Software Radio Systems

Dual SDR Transceivers with 500 MHz A/D, 800 MHz D/A, and Virtex-5 FPGAs

Model 7158 PMC/XMC • Model 7258 6U cPCI • Model 7358 3U cPCI • Model 7658 PCI
Model 7758 Full-length PCIe • Model 7858 Half-length PCIe • Model 5358 3U VPX

Model 7158 is a dual high-speed data converter suitable for connection as the HF or IF input of a communications system. It features two 500 MHz 12-bit A/Ds, a digital upconverter with two 800 MHz 16-bit D/As, and two Virtex-5 FPGAs. Model 7158 uses the popular PMC format and supports the VITA 42 XMC standard for switched fabric interfaces.

The Model 7158 architecture includes two Virtex-5 FPGAs. The first FPGA is used primarily for signal processing while the second one is dedicated to board interfaces. All of the board's data and control paths are accessible by the FPGAs, enabling factory installed functions such as data multiplexing, channel selection, data packing, gating, triggering and SDRAM memory control.

Two independent 256 MB banks of DDR2 SDRAM are available to the signal processing FPGA. Built-in memory functions include an A/D data transient capture mode with pre- and post-triggering. All memory banks can be easily accessed through the PCI-X interface.

A 5-channel DMA controller and 64 bit / 100 MHz PCI-X interface assures efficient transfers to and from the module.

Two 4X switched serial ports implemented with the Xilinx Rocket I/O interfaces, connect the FPGA to the XMC connector with two 2.5 GB/sec data links to the carrier board.

A dual bus system timing generator allows for sample clock synchronization to an external system reference. It also supports large, multichannel applications where the relative phases must be preserved.

Versions of the 7158 are also available as a PCIe full-length board (Models 7758 and 7758D dual density), PCIe half-length board (Model 7858), PCI board (Model 7658), 6U cPCI (Models 7258 and 7258D dual density), 3U cPCI (Model 7358), and 3U VPX (Model 5358). All these products have similar features.
Putting FPGAs to Work in Software Radio Systems

Model 71620 is a member of the Cobalt® family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution. It includes three 200 MHz, 16-bit A/Ds, a DUC with two 800 MHz, 16-bit D/As and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71620 includes general purpose and gigabit serial connectors for application-specific I/O.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71620 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

Multiple 71620's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules. The architecture supports up to four memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Versions of the 71620 are also available as a PCIe half-length board (Model 78620), 3U VPX (Model 53620), 6U cPCI (Models 72620 and 74620 dual density), and 3U cPCI (Model 73620).
Model 71621 is a member of the Cobalt family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter based on the Model 71620 described in the previous page, it includes factory-installed IP cores to enhance the performance of the 71620 and address the requirements of many applications.

The 71621 factory-installed functions include three A/D acquisition and one D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The 71621 also features a complete beamforming subsystem. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The power meters present average power measurements for each DDC core output in easy-to-read registers. A threshold detector automatically sends an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

Versions of the 71621 are also available as a PCIe half-length board (Model 78621), 3U VPX (Model 53621), 6U cPCI (Models 72621 and 74621 dual density), and 3U cPCI (Model 73621).
Model 78630 is a member of the Cobalt family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. It includes 1 GHz, 12-bit A/D, 1 GHz, 16-bit D/A converters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78630 includes optional general purpose and gigabit serial card connectors for application-specific I/O protocols.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 78630 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

Multiple 78630’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. The architecture supports up to four memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Versions of the 78630 are also available as an XMC module (Model 71630), 3U VPX (Model 53630), 6U cPCI (Models 72630 and 74630 dual density), and 3U cPCI (Model 73630).
Models 72640, 73640 and 74640 are members of the Cobalt family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71640 XMC modules mounted on a cPCI carrier board. These models include one or two 3.6 GHz, 12-bit A/D converters and four or eight banks of memory.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The factory-installed functions of these models include one or two A/D acquisition IP modules. In addition, IP modules for DDR3 memories, controllers for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

The front end accepts analog HF or IF inputs on a pair of front panel SSMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz. The ADC12D1800 provides a programmable 15-bit gain adjustment allowing these models to have a full scale input range of +2 dBm to +4 dBm.

Model 72640 is a 6U cPCI board, while Model 73640 is a 3U cPCI board; Model 74640 is a dual density 6U cPCI board. Also available is an XMC module (Model 71640), PCIe half-length board (Model 78640), and 3U VPX (Model 53640).
Model 53650 is a member of the Cobalt family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A two-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. The 53650 includes two 500 MHz 12-bit A/Ds, one DUC, two 800 MHz 16-bit D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53650 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

Multiple 53650’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. The architecture supports up to four memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Versions of the 53650 are also available as an XMC module (Model 71650), as a PCIe half-length board (Model 78650), 6U cPCI (Models 72650 and 74650 dual density), and 3U cPCI (Model 73650).
Models 72651, 73651 and 74651 are members of the Cobalt family of high performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71651 XMC modules mounted on a cPCI carrier board. These models include two or four A/Ds, two or four multiband DDCs, one or two DUCs, two or four D/As and three or six banks of memory.

These models feature two or four A/D Acquisition IP modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP module in loopback mode.

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two or four different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

In addition to the DDCs, these models feature one or two complete beamforming subsystems. Each DDC core contains programable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output in easy-to-read registers.

Model 72651 is a 6U cPCI board, while Model 73651 is a 3U cPCI board; Model 74651 is a dual density 6U cPCI board. Also available is an XMC module (Model 71651), PCIe half-length board (Model 78651), and 3U VPX (Model 53651).
Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71660 factory-installed functions include four A/D acquisition IP modules. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

Multiple 71660’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules. The architecture supports up to four memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Versions of the 71660 are also available as a PCIe half-length board (Model 78660), 3U VPX (Model 53660), 6U cPCI (Models 72660 and 74660 dual density), and 3U cPCI (Model 73660).
Model 71661 is a member of the Cobalt family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter based on the Model 71660 described in the previous page, it includes factory-installed IP cores to enhance the performance of the 71620 and address the requirements of many applications.

The 71661 factory-installed functions include four A/D acquisition IP modules. Each of the four acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The 71661 also features a complete beamforming subsystem. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The power meters present average power measurements for each DDC core output in easy-to-read registers. A threshold detector automatically sends an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

For larger systems, multiple 71661's can be chained together via the built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector.

Versions of the 71661 are also available as a PCIe half-length board (Model 78661), 3U VPX (Model 53661), 6U cPCI (Models 72661 and 74661 dual density), and 3U cPCI (Model 73661).
Model 78662 is a member of the Cobalt family of high performance PCIe boards based on the Xilinx Virtex-6 FPGA. Based on the Model 71660 presented previously, this four-channel, high-speed data converter with programmable DDCs is suitable for connection to HF or IF ports of a communications or radar system.

The 78662 factory-installed functions include four A/D acquisition IP modules. Each of the four acquisition IP modules contains a powerful, programmable 8-channel DDC IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, voltage and temperature monitoring, and a PCIe interface complete the factory-installed functions.

Each of the 32 DDC channels has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. All of the 8 channels within a bank share a common decimation setting ranging from 16 to 8192 programmable in steps of eight. Each 8-channel bank can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of $f_s/N$. Any number of channels can be enabled within each bank, selectable from 0 to 8. Multiple 78662’s can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Versions of the 78662 are also available as an XMC module (Model 71662), 3U VPX (Model 53662), 6U cPCI (Models 72662 and 74662 dual density), and 3U cPCI (Model 73662).
Model 71670 is a member of the Cobalt family of high performance XMC modules based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications. It includes four D/As, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71670 includes general purpose and gigabit serial connectors for application-specific I/O.

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71670 factory-installed functions include four D/A waveform playback IP modules, to support waveform generation through the D/A converters. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71670 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

The Model 71670 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked list controllers support waveform generation to the four D/As from tables stored in either on-board memory or off-board host memory.

Versions of the 71670 are also available as a PCIe half-length board (Model 78670), 3U VPX (Model 53670), 6U cPCI (Models 72679 and 74670 dual density), and 3U cPCI (Model 73670).
Model 53690 is a member of the Cobalt family of high performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A 2-Channel high-speed data converter, it is suitable for connection directly to the RF port of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution. The Model 53690 includes an L-Band RF tuner, two 200 MHz, 16-bit A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board’s data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 53690 factory-installed functions include two A/D acquisition IP modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions.

A front panel connector accepts L-Band signals between 925 MHz and 2175 MHz from an antenna LNB. A Maxim MAX2112 tuner directly converts these signals to baseband using a broadband I/Q downconverter. The device includes an RF variable-gain LNA (low-noise amplifier), a PLL synthesized local oscillator, quadrature (I + Q) downconverting mixers, baseband lowpass filters and variable-gain baseband amplifiers.

Versions of the 53690 are also available as an XMC module (Model 71690), as a PCIe half-length board (Model 78690), 6U cPCI (Models 72690 and 74690 dual density), and 3U cPCI (Model 73690).
Model 71760 is a member of the Onyx™ family of high performance XMC modules based on the Xilinx Virtex-7 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71760 includes general purpose and gigabit serial connectors for application-specific I/O.

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board’s analog interfaces. The 71760 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71760 to operate as a complete turnkey solution without the need to develop any FPGA IP.

The 71760 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module’s DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

Versions of the 71760 are also available as a PCIe half-length board (Model 78760), 3U VPX (Model 53760), 6U cPCI (Models 72760 and 74760 dual density), and 3U cPCI (Model 73760).
215 MHz, 12-bit A/D with Wideband DDCs - VME/VXS

The Model 6821 is a 6U single slot board with the AD9430 12-bit, 215 MHz A/D converter.

Capable of digitizing input signal bandwidths up to 100 MHz, it is ideal for wideband applications including radar and spread spectrum communication systems.

The sampling clock can be supplied either from a front panel input or from an internal crystal oscillator. Data from the A/D converter flows into two Xilinx Virtex-II Pro FPGAs where optional signal processing functions can be performed. The size of the FPGAs can range from the XC2VP20 to the XC2VP50.

Because the sampling rate is well beyond conventional ASIC digital downconverters, none are included on the board.

Instead, the Pentek GateFlow IP Core 422 Ultra Wideband Digital Downconverter can be factory-installed in one or both of the FPGAs to perform this function.

Two 128 MB SDRAMs, one for each FPGA, support large memory applications such as swinging buffers, digital filters, DSP algorithms, and digital delay lines for tracking receivers.

Either two or four FPDP-II ports connect the FPGAs to external digital destinations such as processor boards, memory boards or storage devices.

A VMEbus interface supports configuration of the FPGAs over the backplane and also provides data and control paths for runtime applications. A VXS interface is optionally available.

This Model is available in commercial as well as conduction-cooled versions.
The Model 6822 is a 6U single slot VME board with two AD9430 12-bit 215 MHz A/D converters.

Capable of digitizing input signal bandwidths up to 100 MHz, it is ideal for wideband applications including radar and spread spectrum communication systems.

The sampling clock can be supplied either from a front panel input or from an internal crystal oscillator. Data from each A/D converter flows into a Xilinx Virtex-II Pro FPGA where optional signal processing functions can be performed. The size of the FPGAs can range from the XC2VP20 to the XC2VP50.

Because the sampling rate is well beyond conventional ASIC digital downconverters, none are included on the board.

Instead, the Pentek GateFlow IP Core 422 Ultra Wideband Digital Downconverter can be factory-installed in one or both of the FPGAs to perform this function.

Two 128 MB SDRAMs, one for each FPGA, support large memory applications such as swinging buffers, digital filters, DSP algorithms, and digital delay lines for tracking receivers.

Either two or four FPDP-II ports connect the FPGAs to external digital destinations such as processor boards, memory boards or storage devices.

A VMEbus interface supports configuration of the FPGAs over the backplane and also provides data and control paths for runtime applications. A VXS interface is optionally available.

This Model is available in commercial as well as conduction-cooled versions.
The Model 6826 is a 6U single slot VME board with two Atmel AT84AS008 10-bit 2 GHz A/D converters.

Capable of digitizing input signals at sampling rates up to 2 GHz, it is ideal for extremely wideband applications including radar and spread spectrum communication systems. The sampling clock is an externally supplied sinusoidal clock at a frequency from 200 MHz to 2 GHz.

Data from each of the two A/D converters flows into an innovative dual-stage demultiplexer that packs groups of eight data samples into 80-bit words for delivery to the Xilinx Virtex-II Pro XC2VP70 FPGA at one eighth the sampling frequency. This advanced circuit features the Atmel AT84CS001 demultiplexer which represents a significant improvement over previous technology.

Because the sampling rate is well beyond conventional digital downconverters, none are included on the board. A very high-speed digital downconverter IP core for the Model 6826 can be developed for a customer who is interested in one.

The customer will be able to incorporate this core into the Model 6826 by ordering it as a factory-installed option.

Two 512 MB or 1 GB SDRAMs, support large memory applications such as swinging buffers, digital filters, DSP algorithms, and digital delay lines for tracking receivers.

Either two or four FPDP-II ports connect the FPGA to external digital destinations such as processor boards, memory boards or storage devices.

A VMEbus interface supports configuration of the FPGA over the backplane and also provides data and control paths for runtime applications. A VXS interface is optionally available.

This Model is also available in a single-channel version and in commercial as well as conduction-cooled versions.
Model 6890 Clock, Sync and Gate Distribution Board synchronizes multiple Pentek I/O boards within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP and software radio applications. Up to eight boards can be synchronized using the 6890, each receiving a common clock of up to 2.2 GHz along with timing signals that can be used for synchronizing, triggering and gating functions.

Clock signals are applied from an external source such as a high performance sine wave generator. Gate and sync signals can come from an external source, or from one supported board set to act as the master.

The 6890 accepts clock input at +10 dBm to +14 dBm with a frequency range from 800 MHz to 2.2 GHz and uses a 1:2 power splitter to distribute the clock. The first output of this power splitter sends the clock signal to a 1:8 splitter for distribution to up to eight boards using SMA connectors. The second output of the 1:2 power splitter feeds a 1:2 buffer which distributes the clock signal to both the gate and synchronization circuits.

The 6890 features separate inputs for gate/trigger and sync signals with user-selectable polarity. Each of these inputs can be TTL or LVPECL. Separate Gate Enable and Sync Enable inputs allow the user to enable or disable these circuits using an external signal.

A programmable delay allows the user to make timing adjustments on the gate and sync signals before they are sent to an LVPECL buffer. A bank of eight MMCX connectors at the output of each buffer delivers signals to up to eight boards.

A 2:1 multiplexer in each circuit allows the gate/trigger and sync signals to be registered with the input clock signal before output, if desired.

Sets of input and output cables for two to eight boards are available from Pentek.
Model 6891 System Synchronizer and Distribution Board synchronizes multiple Pentek I/O modules within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP and software radio applications.

Up to eight modules can be synchronized using the 6891, each receiving a common clock up to 500 MHz along with timing signals that can be used for synchronizing, triggering and gating functions. For larger systems, up to eight 6891’s can be linked together to provide synchronization for up to 64 I/O modules producing systems with up to 256 channels.

Model 6891 accepts three TTL input signals from external sources: one for clock, one for gate or trigger and one for a synchronization signal. Two additional inputs are provided for separate gate and sync enable signals. Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. Alternately, a Sync Bus connector accepts LVPECL inputs from any compatible Pentek products to drive the clock, sync and gate/trigger signals.

The 6891 provides eight front panel Sync Bus output connectors, compatible with a wide range of Pentek I/O modules. The Sync Bus is distributed through ribbon cables, simplifying system design. The 6891 accepts clock input at +10 dBm to +14 dBm with a frequency range from 1 kHz to 800 MHz. This clock is used to register all sync and gate/trigger signals as well as providing a sample clock to all connected I/O modules.

A programmable delay allows the user to make timing adjustments on the gate and sync signals before they are sent to an LVPECL buffer for output through the Sync Bus connectors.
Putting FPGAs to Work in Software Radio Systems

Multifrequency Clock Synthesizer

Model 7190 PMC • Model 7290 6U cPCI • Model 7390 3U cPCI • Model 7690 PCI
Model 7790 Full-length PCIe • Model 7890 Half-length PCIe • Model 5390 3U VPX

Figure 49

Model 7190 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from on-board quad VCXOs and can be phase-locked to an external reference signal.

The 7190 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to generate one of four frequencies between 50 MHz and 700 MHz.

The CDC7005 can output the selected frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005’s can output up to five frequencies each. The 7190 can be programmed to route any of these 20 frequencies to the module’s five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference of 5 MHz to 100 MHz.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs. With four independent quad VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7190’s can be used and phase-locked with the 5 MHz to 100 MHz system reference.

Versions of the 7190 are also available as a PCIe full-length board (Models 7790 and 7790D dual density), PCIe half-length board (Model 7890), 3U VPX board (Model 5390), PCI board (Model 7690), 6U cPCI (Models 7290 and 7290D dual density), or 3U cPCI (Model 7390).
Model 7191 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from programmable VCXOs and can be phase-locked to an external reference signal.

The 7191 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to a desired frequency between 50 MHz and 700 MHz with 32-bit tuning resolution.

The CDC7005 can output the programmed frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005’s can output up to five frequencies each. The 7191 can be programmed to route any of these 20 frequencies to the module’s five output drivers.

The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference of 5 MHz to 100 MHz.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs. With four programmable VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7191’s can be used and phase-locked with the 5 MHz to 100 MHz system reference.

Versions of the 7191 are also available as a PCIe full-length board (Models 7791 and 7791D dual density), PCIe half-length board (Model 7891), 3U VPX board (Model 5391), PCI board (Model 7691), 6U cPCI (Models 7291 and 7291D dual density), or 3U cPCI (Model 7391).
The Model 7192 High-Speed Synchronizer and Distribution Board synchronizes multiple Pentek Cobalt or Onyx modules within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP, and software radio applications. Up to four modules can be synchronized using the 7192, with each receiving a common clock along with timing signals that can be used for synchronizing, triggering and gating functions.

Model 7192 provides three front panel MMCX connectors to accept input signals from external sources: one for clock, one for gate or trigger and one for a synchronization signal. Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. In addition to the MMCX connector, a reference clock can be accepted through the first front panel µSync output connector, allowing a single Cobalt or Onyx board to generate the clock for all subsequent boards in the system.

The 7192 provides four front panel µSync output connectors, compatible with a range of high-speed Pentek Cobalt and Onyx modules. The µSync signals include a reference clock, gate/trigger and sync signals and are distributed through matched cables, simplifying system design. The 7192 features a calibration output specifically designed to work with the 71640 or 71740 3.6 GHz A/D module and provide a signal reference for phase adjustment across multiple D/As.

The 7192 supports all high-speed models in the Cobalt family including the 71630 1 GHz A/D and D/A XMC, the 71640 3.6 GHz A/D XMC and the 71670 Four-channel 1.25 GHz, 16-bit D/A XMC. The 7192 will also support high-speed models in the Onyx family as they become available.

Versions of the 7192 are also available as a PCIe half-length board (Model 7892), 3U VPX (Model 5392), 6U cPCI (Models 7292 and 7492 dual density), and 3U cPCI (Model 7392).
Model 7893 System Synchronizer and Distribution Board synchronizes multiple Pentek Cobalt and Onyx boards within a system. It enables synchronous sampling, playback and timing for a wide range of multichannel high-speed data acquisition, DSP and software radio applications.

Up to eight boards can be synchronized using the 7893, each receiving a common clock up to 800 MHz along with timing signals that can be used for synchronizing, triggering and gating functions. For larger systems, up to eight 7893s can be linked together to provide synchronization for up to 64 Cobalt or Onyx boards.

The Model 7893 provides four front panel SMA connectors to accept LVTTL input signals from external sources: two for Sync/PPS and one for Gate/Trigger. In addition to the synchronization signals, a front panel SMA connector accepts sample clocks up to 800 MHz or, in an alternate mode, accepts a 10 MHz reference clock to lock an on-board VCXO sample clock source.

The 7893 provides eight timing bus output connectors for distributing all needed timing and clock signals to the front panels of Cobalt and Onyx boards via ribbon cables. The 7893 locks the Gate/Trigger and Sync/PPS signals to the system’s sample clock. The 7893 also provides four front panel SMA connectors for distributing sample clocks to other boards in the system.

The 7893 can accept a clock from either the front panel SMA connector or from the timing bus input connector. A programmable on-board VCXO clock generator can be locked to a user-supplied, 10 MHz reference.

The 7893 supports a wide range of products in the Cobalt family including the 78620 and 78621 three-channel A/D 200 MHz transceivers, the 78650 and 78651 two-channel A/D 500 MHz transceivers, the 78660, 78661 and 78662 four-channel 200 MHz A/Ds, and the 78690 L-Band RF Tuner. The 7893 also supports the Onyx 78760 four-channel 200 MHz A/D and will support all complementary models in the Onyx family as they become available.
Model 9190 Clock and Sync Generator synchronizes multiple Pentek I/O modules within a system to provide synchronous sampling and timing for a wide range of high-speed, multichannel data acquisition, DSP and software radio applications. Up to 80 I/O modules can be driven from the Model 9190, each receiving a common clock and up to five different timing signals which can be used for synchronizing, triggering and gating functions.

Clock and timing signals can come from six front panel SMA user inputs or from one I/O module set to act as the timing signal master. (In this case, the master I/O module will not be synchronous with the slave modules due to delays through the 9190.) Alternately, the master clock can come from a socketed, user-replaceable crystal oscillator within the Model 9190.

Buffered versions of the clock and five timing signals are available as outputs on the 9190’s front panel SMA connectors.

Model 9190 is housed in a line-powered, 1.75 in. high metal chassis suitable for mounting in a standard 19 in. equipment rack, either above or below the cage holding the I/O modules.

Separate cable assemblies extend from openings in the front panel of the 9190 to the front panel clock and sync connectors of each I/O module. Mounted between two standard rack-mount card cages, Model 9190 can drive a maximum of 80 clock and sync cables, 40 to the card cage above and 40 to the card cage below. Fewer cables may be installed for smaller systems.
Model 9192 Rackmount High-Speed System Synchronizer Unit synchronizes multiple Pentek Cobalt or Onyx modules within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP, and software radio applications. Up to twelve boards can be synchronized using the 9192, each receiving a common clock along with timing signals that can be used for synchronizing, triggering, and gating functions.

Model 9192 provides four rear panel SMA connectors to accept input signals from external sources: two for clock, one for gate or trigger and one for a synchronization signal. Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. In addition to the SMA connector, a reference clock can be accepted through the first rear panel µSync output connector, allowing a single Cobalt or Onyx board to generate the clock for all subsequent boards in the system.

The 9192 provides four rear panel µSync output connectors, compatible with a range of high-speed Pentek Cobalt and Onyx boards. The µSync signals include a reference clock, gate/trigger and sync signals and are distributed through matched cables, simplifying system design.

The 9192 features twelve calibration outputs specifically designed to work with the 71640 or 71740 3.6 GHz A/D module and provide a signal reference for phase adjustment across multiple D/As.

The 9192 allows programming of operation parameters including: VCXO frequency, clock dividers, and delays that allow the user to make timing adjustments on the gate and sync signals. These adjustments are made before they are sent to buffers for output through the µSync connectors.

The 9192 supports all high-speed models in the Cobalt family including the 71630 1 GHz A/D and D/A XMC, the 71640 3.6 GHz A/D XMC and the 71670 Four-channel 1.25 GHz, 16-bit D/A XMC. The 9192 will also support high-speed models in the Onyx family as they become available.
The Talon™ RTS 2706 is a turnkey, multiband recording and playback system for recording and reproducing high-bandwidth signals. The RTS 2706 uses 16-bit, 200 MHz A/D converters and provides sustained recording rates up to 1600 MB/sec in four-channel configuration.

The RTS 2706 uses Pentek’s high-powered Virtex-6-based Cobalt® modules, that provide flexibility in channel count, with optional DDC (Digital Downconversion) capabilities. Optional 16-bit, 800 MHz D/A converters with DUC (Digital Upconversion) allow real-time reproduction of recorded signals.

A/D sampling rates, DDC decimations and bandwidths, D/A sampling rates and DUC interpolations are among the GUI-selectable system parameters, providing a fully-programmable system capable of recording and reproducing a wide range of signals.

Included with this system is Pentek’s SystemFlow recording software. Optional GPS time and position stamping allows the user to record this critical signal information.

Built on a Windows® 7 Professional workstation with high performance Intel® Core™ i7 processor the RTS 2706 allows the user to install post processing and analysis tools to operate on the recorded data. The system records data to the native NTFS file system, providing immediate access to the recorded data.

The RTS 2706 is configured in a 4U 19” rack-mountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel. Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates. All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC.
Ultra Wideband One- or Two-Channel RF/IF, 3.2 GS/sec Rackmount Recorder

The Talon RTS 2709 is a turnkey system used for recording extremely high-bandwidth signals. The RTS 2709 uses a 12-bit, 3.6 GHz A/D converter and can provide sustained recording rates up to 3,200 MB/sec. It can be configured as a one- or two-channel system and can record sampled data, packed as 8-bit wide consecutive samples, or as 16-bit wide consecutive samples (12-bit digitized samples residing in the 12 MSBs of the 16-bit word.)

The RTS 2709 uses Pentek’s high-powered Virtex-6-based Cobalt boards that provide the data streaming engine for the high-speed A/D converter. Channel and packing modes as well as gate and trigger settings are among the GUI-selectable system parameters, providing complete control over this ultra wideband recording system.

Optional GPS time and position stamping allows the user to capture this information in the header of each data file.

The RTS 2709 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple means to configure and control the system. Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

SystemFlow also includes signal viewing and analysis tools that allow the user to monitor the signal prior to, during, and after a recording session.

Built on a Windows 7 Professional workstation, the RTS 2709 allows the user to install post processing and analysis tools to operate on the recorded data. The RTS 2709 records data to the native NTFS file system that provides immediate access to the recorded data. The RTS 2709 is configured in a 4U 19" rack-mountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel.
The Talon RTS 2715 is a complete turnkey recording system for storing one or two 10 gigabit Ethernet (10 GbE) streams. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and supports both TCP and UDP protocols.

Two rear panel SFP+ LC connectors for 850 nm multi-mode or single-mode fibre cables, or CX4 connectors for copper twinax cables accommodate all popular 10 GbE interfaces.

Optional GPS time and position stamping accurately identifies each record in the file header.

The RTS 2715 includes the SystemFlow Recording Software that provides a simple and intuitive means to configure and control the system. Custom configurations can be stored as profiles and later loaded as needed, allowing the user to select preconfigured settings with a single click.

Built on a server-class Windows 7 Professional workstation, the RTS 2715 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTS 2715 records data to the native NTFS file system, providing immediate access to the recorded data.

The RTS 2715 is configured in a 5U 19” rack-mountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel. The 24 hot-swappable HDD’s provide a storage capacity of 20 TB.

Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates. All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC.
The Talon RTS 2716 is a complete turnkey recording system capable of recording and playing multiple serial FPDP data streams. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and is fully compatible with the VITA 17.1 specification. Using highly-optimized disk storage technology, the system achieves aggregate recording rates up to 2 GB/sec.

The RTS 2716 can be populated with up to eight SFP connectors supporting serial FPDP over copper, single-mode, or multi-mode fiber, accommodate all popular serial FPDP interfaces. It is capable of both receiving and transmitting data over these links and supports real-time data storage to disk.

Programmable modes include flow control in both receive and transmit directions, CRC support, and copy/loop modes. The system is capable of handling 1.0625, 2.125 and 2.5 GBAud link rates supporting data transfer rates of up to 247 MBytes/sec per serial FPDP link.

Built on a server-class Windows 7 Professional workstation, the RTS 2716 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTS 2716 records data to the native NTFS file system, providing immediate access to the recorded data.

The RTS 2716 includes the SystemFlow Recording Software, which features a Windows-based GUI that provides a simple and intuitive means to configure and control the system.
The Talon RTR 2726 is a turnkey, multiband recording and playback system designed to operate under conditions of shock and vibration. It allows the user to record and reproduce high-bandwidth signals with a lightweight, portable and rugged package. The RTR 2726 provides sustained recording rates of up to 1600 MB/sec in a four-channel system and is ideal for the user who requires both portability and solid performance in a compact recording system.

The RTR 2726 is supplied in a small footprint portable package measuring only 16.9” W x 9.5” D x 13.4” H and weighing just 30 pounds. With measurements similar to a small briefcase, this portable workstation includes an Intel Core i7 processor, a high-resolution 17” LCD monitor, and a high-performance SATA RAID controller.

At the heart of the RTR 2726 are Pentek Cobalt Series Virtex-6 software radio boards featuring A/D and D/A converters, DDCs (Digital Downconverters), DUCs (Digital Upconverters), and complementary FPGA IP cores. This architecture allows the system engineer to take full advantage of the latest technology in a turnkey system. Optional GPS time and position stamping allows the user to record this critical signal information.

Built on a Windows 7 Professional workstation, the RTR 2726 allows the user to install post processing and analysis tools to operate on the recorded data. The RTR 2726 records data to the native NTFS file system, providing immediate access to the recorded data.

The eight hot-swappable SSDs provide a storage capacity of up to 4 TB. The drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Because SSDs operate reliably under conditions of vibration and shock, the RTR 2726 performs well in ground, shipborne and airborne environments.
The Talon RTR 2736 is a complete turnkey recording system designed to operate under conditions of shock and vibration. It records and plays back multiple serial FPDP data streams in a rugged, lightweight portable package. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and is fully compatible with the VITA 17.1 specification. Using highly-optimized disk storage technology, the system achieves aggregate recording rates up to 1600 MB/sec.

The RTR 2736 can be populated with up to eight SFP connectors supporting serial FPDP over copper, single-mode, or multi-mode fiber, accommodate all popular serial FPDP interfaces. It is capable of both receiving and transmitting data over these links and supports real-time data storage to disk. Optional GPS time and position stamping allows the user to mark the beginning of a recording in the recording file’s header.

The RTR 2736 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple and intuitive means to configure and control the system. Custom configurations can be stored as profiles and later loaded as needed, allowing the user to select preconfigured settings with a single click.

The RTR 2736 is configured in a portable, lightweight chassis with eight hot-swap SSDs, front panel USB ports and I/O connections on the side panel. It is built on an extremely rugged, 100% aluminum alloy unit, reinforced with shock absorbing rubber corners and an impact-resistant protective glass. Using vibration and shock resistant SSDs, the RTR 2736 is designed to reliably operate as a portable field instrument in harsh environments.

The eight hot-swappable SSDs provide storage capacities of up to 3.8 TB. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data.
The Talon RTR 2746 is a turnkey multiband recording and playback system designed to operate under conditions of shock and vibration. The RTR 2746 is intended for military, airborne and UAV applications requiring a rugged system. With scalable A/Ds, D/A and SSD (solid-state drive) storage, the RTR 2746 can be configured to stream data to and from disk at rates as high as 1600 MB/sec.

The RTR 2746 uses Pentek’s high-powered Virtex-6-based Cobalt boards, that provide flexibility in channel count with optional digital downconversion capabilities. Optional 16-bit, 800 MHz D/A converters with digital upconversion allow real-time reproduction of recorded signals.

A/D sampling rates, DDC decimations and bandwidths, D/A sampling rates, and DUC interpolations are among the GUI-selectable system parameters, providing a fully programmable system.

The 24 hot-swappable SSD’s provide storage capacity of up to 12 TB. The drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Because SSDs operate reliably under conditions of vibration and shock, the RTR 2746 performs well in ground, shipborne and airborne environments.

The RTR 2746 is configured in a 4U 19” rugged rack-mountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel.

All recorder chassis are connected via Ethernet and can be controlled from a single GUI either locally or from a remote PC. Multiple RAID levels, including 0, 1, 5, 6, 10, and 50, provide a choice for the required level of redundancy.

Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates.
Putting FPGAs to Work in Software Radio Systems

Products

Ultra Wideband One- or Two-Channel RF/IF, 3.2 GS/sec Rugged Rackmount Recorder

![Model RTR 2749 Diagram]

Designed to operate under conditions of shock and vibration, the Talon RTS 2749 is a turnkey system used for recording extremely high-bandwidth signals. The RTS 2749 uses a 12-bit, 3.6 GHz A/D converter and can provide sustained recording rates up to 3,200 MB/sec. It can be configured as a one- or two-channel system and can record sampled data, packed as 8-bit wide consecutive samples, or as 16-bit wide consecutive samples (12-bit digitized samples residing in the 12 MSBs of the 16-bit word.)

The RTS 2749 uses Pentek’s high-powered Virtex-6-based Cobalt boards that provide the data streaming engine for the high-speed A/D converter. Channel and packing modes as well as gate and trigger settings are among the GUI-selectable system parameters, providing complete control over this ultra wideband recording system. Optional GPS time and position stamping allows the user to capture this information in the header of each data file.

The RTS 2749 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple means to configure and control the system. Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click. SystemFlow also includes signal viewing and analysis tools that allow the user to monitor the signal prior to, during, and after a recording session.

Built on a Windows 7 Professional workstation, the RTS 2749 allows the user to install post processing and analysis tools to operate on the recorded data. The hot-swappable SSDs provide a storage capacity of up to 20 TB. The drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Because SSDs operate reliably under conditions of vibration and shock, the RTR 2749 performs well in ground, shipborne and airborne environments.
Putting FPGAs to Work in Software Radio Systems

Two-Channel 10 Gigabit Ethernet Rugged Rackmount Recorder

Model RTR 2755

Designed to operate under conditions of shock and vibration, the Talon RTR 2755 is a complete turnkey recording system for storing one or two 10 gigabit Ethernet (10 GbE) streams. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and supports both TCP and UDP protocols.

Using highly-optimized solid-state drive storage technology, the system guarantees loss-free performance at aggregate recording rates up to 2 GB/sec.

Two rear panel SFP+ LC connectors for 850 nm multi-mode or single-mode fibre cables, or CX4 connectors for copper twinax cables accommodate all popular 10 GbE interfaces.

Optional GPS time and position stamping accurately identifies each record in the file header.

The RTR 2755 includes the SystemFlow Recording Software that provides a simple and intuitive means to configure and control the system. Custom configurations can be stored as profiles and later loaded as needed, allowing the user to select preconfigured settings with a single click.

Built on a server-class Windows 7 Professional workstation, the RTR 2755 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTR 2755 records data to the native NTFS file system, providing immediate access to the recorded data.

Because SSDs operate reliably under conditions of vibration and shock, the RTR 2755 performs well in ground, shipborne and airborne environments. The twelve hot-swappable SSD’s provide a storage capacity of up to 3 TB. The drives can be easily removed or exchanged during or after a mission to retrieve recorded data.
Designed to operate under conditions of shock and vibration, the Talon RTR 2756 is a complete turnkey recording system capable of recording and playing multiple serial FPDP data streams. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and is fully compatible with the VITA 17.1 specification. Using highly-optimized disk storage technology, the system achieves aggregate recording rates up to 2 GB/sec.

The RTR 2756 can be populated with up to eight SFP connectors supporting serial FPDP over copper, single-mode, or multi-mode fiber, accommodate all popular serial FPDP interfaces. It is capable of both receiving and transmitting data over these links and supports real-time data storage to disk.

The RTR 2756 includes the SystemFlow Recording Software that provides an intuitive means to control the system. Custom configurations can be stored as profiles and later loaded as needed, allowing the user to select preconfigured settings with a single click.

Built on a server-class Windows 7 Professional workstation, the RTR 2756 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTR 2756 records data to the native NTFS file system, providing immediate access to the recorded data.

Because SSDs operate reliably under conditions of vibration and shock, the RTR 2756 performs well in ground, ship and airborne environments. Configurable with as many as 40 hot-swappable SSDs, the RTR 2756 can provide storage capacities of up to 19 TB in a rugged 4U chassis. Drives can be easily removed or exchanged during or after a mission to retrieve recorded data. Optional GPS time and position stamping allows the user to mark the beginning of a recording in the recording file's header.
The Pentek SystemFlow® Recording Software provides a rich set of function libraries and tools for controlling all Pentek RTS real-time data acquisition and recording instruments. SystemFlow software allows developers to configure and customize system interfaces and behavior.

The Recorder Interface includes configuration, record, playback and status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperatures and voltage levels.

The Hardware Configuration Interface provides entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

The SystemFlow Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual annotated cursors to mark and measure points of interest, the SystemFlow Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.
Shown above is a 2-channel recording and playback system utilizing the Pentek Cobalt 78651 PCIe board. The 78651 samples two input channels at up to 500 mega-samples per second, thereby accommodating input signals with up to 200 MHz bandwidth.

Factory-installed in the FPGA is a powerful 2-channel DDC (Digital Downconverter) IP core. Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to \( f_s \), where \( f_s \) is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of \( 0.8 \times f_s/N \), where \( N \) is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of \( f_s/N \).

A TI DAC5688 DUC (Digital Upconverter) and D/A accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and dual D/A stages.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to any IF center frequency up to 360 MHz. It delivers real or quadrature (I+Q) analog outputs to the dual 16-bit D/A converter. Analog output is through a pair of front panel SSMC connectors. If translation is disabled, the DAC5688 acts as a dual interpolating 16-bit D/A with output sampling rates up to 800 MHz.

Built on a Windows 7 Professional workstation with high performance Intel® Core™ i7 processor this system allows the user to install post processing and analysis tools to operate on the recorded data. The system records data to the native NTFS file system, providing immediate access to the recorded data.

Included with this system is Pentek’s SystemFlow recording software. Optional GPS time and position stamping allows the user to record this critical signal information.
Shown above is a 64-channel recording system utilizing two Pentek Cobalt 78662 PCIe boards. The 78662 samples four input channels at up to 200 megasamples per second, thereby accommodating input signals with up to 80 MHz bandwidth.

Factory-installed in the FPGA of each 78662 is a powerful DDC IP core containing 32 channels. Each of the 32 channels has an independent 32-bit tuning frequency setting that ranges from DC to $f_s$, where $f_s$ is the A/D sampling frequency. All of the 8 channels within each bank share a common decimation setting that can range from 16 to 8192, programmable in steps of 8. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \times f_s/N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of $f_s/N$. Any number of channels can be enabled within each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within a bank.

An internal timing bus provides all timing and synchronization required by the eight A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

Built on a Windows 7 Professional workstation with high performance Intel® Core™ i7 processor this system allows the user to install post processing and analysis tools to operate on the recorded data. The system records data to the native NTFS file system, providing immediate access to the recorded data.

Included with this system is Pentek’s SystemFlow recording software. Optional GPS time and position stamping allows the user to record this critical signal information.
The Cobalt Model 78690 L-Band RF Tuner targets reception and processing of digitally-modulated RF signals such as satellite television and terrestrial wireless communications. The 78690 requires only an antenna and a host computer to form a complete L-band SDR development platform.

This system receives L-Band signals between 925 MHz and 2175 MHz directly from an antenna. Signals above this range such as C Band, Ku Band and K band can be downconverted to L-Band through an LNB (Low Noise Block) downconverter installed in the receiving antenna.

The Maxim Max2112 L-Band Tuner IC features a low-noise amplifier with programmable gain from 0 to 65 dB and a synthesized local oscillator programmable from 925 to 2175 MHz. The complex analog mixer translates the input signals down to DC. Baseband amplifiers provide programmable gain from 0 to 15 dB in steps of 1 dB. The bandwidth of the baseband lowpass filters can be programmed from 4 to 40 MHz. The Maxim IC accommodates full-scale input levels of -50 dBm to +10 dbm and delivers I and Q complex baseband outputs.

The complex I and Q outputs are digitized by two 200 MHz 16-bit A/D converters operating synchronously.

The Virtex-6 FPGA is a powerful resource for recovering and processing a wide range of signals while supporting decryption, decoding, demodulation, detection, and analysis. It is ideal for intercepting or monitoring traffic in SIGINT and COMINT applications. Other applications that benefit include mobile phones, GPS, satellite terminals, military telemetry, digital video and audio in TV broadcasting satellites, and voice, video and data communications.

This L-Band signal processing system is ideal as a front end for government and military systems. Its small size addresses space-limited applications. Ruggedized options are also available from Pentek with the Models 71690 XMC module and the 53690 OpenVPX board to address UAV applications and other severe environments.

Development support for this system is provided by the Pentek ReadyFlow board support package for Windows, Linux and VxWorks. Also available is the Pentek GateFlow FPGA Design Kit to support custom algorithm development.
Two Model 53661 boards are installed in slots 1 and 2 of an OpenVPX backplane, along with a CPU board in slot 3. Eight dipole antennas designed for receiving 2.5 GHz signals feed RF Tuners containing low noise amplifiers, local oscillators and mixers. The RF Tuners translate the 2.5 GHz antenna frequency signal down to an IF frequency of 50 MHz.

The 200 MHz 16-bit A/Ds digitize the IF signals and perform further frequency downconversion to baseband, with a DDC decimation of 128. This provides I+Q complex output samples with a bandwidth of about 1.25 MHz. Phase and gain coefficients for each channel are applied to steer the array for directionality.

The CPU board in VPX slot 3 sends commands and coefficients across the backplane over two x4 PCIe links, or OpenVPX “fat pipes”.

The first four signal channels are processed in the upper left 53661 board in VPX slot 1, where the 4-channel beamformed sum is propagated through the 4X Aurora Sum Out link across the backplane to the 4X Aurora Sum In port on the second 53661 in slot 2. The 4-channel local summation from the second 53661 is added to the propagated sum from the first board to form the complete 8-channel sum. This final sum is sent across the x4 PCIe link to the CPU card in slot 3.

Assignment of the three OpenVPX 4X links on the Model 53661 boards is simplified through the use of a crossbar switch which allows the 53661 to operate with a wide variety of different backplanes.

Because OpenVPX does not restrict the use of serial protocols across the backplane links, mixed protocol architectures like the one shown are fully supported.
The beamforming demo system is equipped with a Control Panel that runs under Windows on the CPU board. It includes an automatic signal scanner to detect the strongest signal frequency arriving from a test transmitter. This frequency is centered around the 50 MHz IF frequency of the RF downconverter. Once the frequency is identified, the eight DDCs are set accordingly to bring that signal down to 0 Hz for summation.

The control panel software also allows specific hardware settings for all of the parameters for the eight channels including gain, phase, and sync delay. An additional display shows the beam-formed pattern of the array. This display is formed by adjusting the phase shift of each of the eight channels to provide maximum sensitivity across arrival angles from -90° to +90° perpendicular to the plane of the array.

The classic 7-lobe pattern for an ideal 8-element array for a signal arriving at 0° angle (directly in front of the array) is shown above. Below the lobe pattern is a polar plot showing a single vector pointing to the computed angle of arrival. This is derived from identifying the lobe with the maximum response.

An actual plot of a real-life transmitter is also shown for a source directly in front of the display. In this case the perfect lobe pattern is affected by physical objects, reflections, cable length variations and minor differences in the antennas. Nevertheless, the directional information is computed quite well. As the signal source is moved left and right in front of the array, the peak lobe moves with it, changing the computed angle of arrival.

This demo system is available online at Pentek. If you are interested in viewing a live demonstration, please let us know of your interest by clicking on this link: Beamforming Demo.
Putting FPGAs to Work in Software Radio Systems

Summary

DSP Boards for VMEbus

- Freescale Altivec G4 PowerPC
- Texas Instruments C6000 DSPs
- Single, Dual, Quad and Octal Processor versions
- PMC, PMC/XMC, PCI, PCIe, and cPCI peripherals
- VME/VXS platforms

FPGAs and SDR

- **Communications Algorithms**: DDC, DUC, demodulation, decoding, symbol recovery
- **Beamforming**: direction finding, phased array processing, diversity receivers
- **Analysis**: FFTs, decryption, statistical analysis
- **Triggering and Gating**: radar acquisition and control
- **Memory control**: DMA engines, circular buffers
- **Formatting and Packing**: flexible data manipulation for special I/O, packet extraction and formation
- **High-Speed Interfaces**: switched serial fabric interfaces, such as Serial RapidIO, PCI Express

Pentek offers a comprehensive array of VMEbus DSP boards featuring the Altivec G4 PowerPC from Freescale and the TMS320C6000 family of processor products from Texas Instruments.

On-board processor densities range from one to eight DSPs with many different memory and interface options available.

The Models 4205 and 4207 I/O processor boards feature the latest G4 PowerPCs, accept PMC mezzanines and include built-in Fibre Channel interfaces.

The Models 4294 and 4295 processor boards feature four MPC74xx G4 PowerPC processors utilizing the Altivec vector processor capable of delivering several GFLOPS of processing power.

The Models 4292 and 4293 processor boards feature the Texas Instruments latest TMS320C6000 family of fixed-point DSPs that represent a 10-fold increase in processing power over previous designs.

Once again, the ability of the system designer to freely choose the most appropriate DSP processor for each software radio application, facilitates system requirement changes and performance upgrades.

Full software development tools are available for workstations running Windows and Linux with many different development system configurations available.

As we have seen, FPGAs are truly an integral part of the latest generation of software radio products.

Not only are they being used with traditional digital signal processing algorithms but also in the management of data acquisition, buffering, triggering and timing aspects of high-performance real time systems.

With the addition of FPGA technology, dramatic increases in system density have been coupled with a significantly lower cost per channel. Furthermore, FPGA technology allows one to incorporate custom algorithms right at the front end of these systems.

Pentek offers not only a wide range of hardware products featuring the latest FPGAs, but also the FPGA development resources and knowledgeable applications engineers to help you get the most out of these products.

We encourage you to contact your Pentek sales engineers today to discuss your system needs.

And be sure to visit our extensive web site for the latest product and technical information.
The following links provide you with additional information about the Pentek products presented in this handbook: just click on the model number. Links are also provided to other handbooks or catalogs that may be of interest in your software radio development projects.

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>7131</td>
<td>Multiband Receiver - PMC</td>
<td>17</td>
</tr>
<tr>
<td>7231</td>
<td>Multiband Receiver - 6U cPCI</td>
<td>17</td>
</tr>
<tr>
<td>7331</td>
<td>Multiband Receiver - 3U cPCI</td>
<td>17</td>
</tr>
<tr>
<td>7631A</td>
<td>Multiband Receiver - PCI</td>
<td>17</td>
</tr>
<tr>
<td>5331</td>
<td>Multiband Receiver - 3U VPX</td>
<td>17</td>
</tr>
<tr>
<td>7141</td>
<td>Multiband Transceiver with Virtex-II Pro FPGA - PMC/XMC</td>
<td>18</td>
</tr>
<tr>
<td>7141-703</td>
<td>Conduction-cooled Multiband Transceiver with Virtex-II FPGA - PMC/XMC</td>
<td>18</td>
</tr>
<tr>
<td>7241</td>
<td>Multiband Transceiver with Virtex-II Pro FPGA - 6U cPCI</td>
<td>18</td>
</tr>
<tr>
<td>7341</td>
<td>Multiband Transceiver with Virtex-II Pro FPGA - 3U cPCI</td>
<td>18</td>
</tr>
<tr>
<td>7641</td>
<td>Multiband Transceiver with Virtex-II Pro FPGA - PCI</td>
<td>18</td>
</tr>
<tr>
<td>7741</td>
<td>Multiband Transceiver with Virtex-II Pro FPGA - Full-length PCIe</td>
<td>18</td>
</tr>
<tr>
<td>7841</td>
<td>Multiband Transceiver with Virtex-II Pro FPGA - Half-length PCIe</td>
<td>18</td>
</tr>
<tr>
<td>5341</td>
<td>Multiband Transceiver with Virtex-II Pro FPGA - 3U VPX</td>
<td>18</td>
</tr>
<tr>
<td>7141-420</td>
<td>Transceiver w. Dual Wideband DDC and Interpolation Filter - PMC/XMC</td>
<td>19</td>
</tr>
<tr>
<td>7241-420</td>
<td>Transceiver w. Dual Wideband DDC and Interpolation Filter - 6U cPCI</td>
<td>19</td>
</tr>
<tr>
<td>7341-420</td>
<td>Transceiver w. Dual Wideband DDC and Interpolation Filter - 3U cPCI</td>
<td>19</td>
</tr>
<tr>
<td>7641-420</td>
<td>Transceiver w. Dual Wideband DDC and Interpolation Filter - PCI</td>
<td>19</td>
</tr>
<tr>
<td>7741-420</td>
<td>Transceiver w. Dual Wideband DDC and Interpolation Filter - Full-length PCIe</td>
<td>19</td>
</tr>
<tr>
<td>7841-420</td>
<td>Transceiver w. Dual Wideband DDC and Interpolation Filter - Half-length PCIe</td>
<td>19</td>
</tr>
<tr>
<td>5341-420</td>
<td>Transceiver w. Dual Wideband DDC and Interpolation Filter - 3U VPX</td>
<td>19</td>
</tr>
<tr>
<td>7141-430</td>
<td>Transceiver w. 256-Channel Narrowband DDC - PMC/XMC</td>
<td>20</td>
</tr>
<tr>
<td>7241-430</td>
<td>Transceiver w. 256-Channel Narrowband DDC - 6U cPCI</td>
<td>20</td>
</tr>
<tr>
<td>7341-430</td>
<td>Transceiver w. 256-Channel Narrowband DDC - 3U cPCI</td>
<td>20</td>
</tr>
<tr>
<td>7641-430</td>
<td>Transceiver w. 256-Channel Narrowband DDC - PCI</td>
<td>20</td>
</tr>
<tr>
<td>7741-430</td>
<td>Transceiver w. 256-Channel Narrowband DDC - Full-length PCIe</td>
<td>20</td>
</tr>
<tr>
<td>7841-430</td>
<td>Transceiver w. 256-Channel Narrowband DDC - Half-length PCIe</td>
<td>20</td>
</tr>
<tr>
<td>5341-430</td>
<td>Transceiver w. 256-Channel Narrowband DDC - 3U VPX</td>
<td>20</td>
</tr>
<tr>
<td>7142</td>
<td>Multichannel Transceiver with Virtex-4 FPGAs - PMC/XMC</td>
<td>21</td>
</tr>
<tr>
<td>7242</td>
<td>Multichannel Transceiver with Virtex-4 FPGAs - 6U cPCI</td>
<td>21</td>
</tr>
<tr>
<td>7342</td>
<td>Multichannel Transceiver with Virtex-4 FPGAs - 3U cPCI</td>
<td>21</td>
</tr>
<tr>
<td>7642</td>
<td>Multichannel Transceiver with Virtex-4 FPGAs - PCI</td>
<td>21</td>
</tr>
<tr>
<td>7742</td>
<td>Multichannel Transceiver with Virtex-4 FPGAs - Full-length PCIe</td>
<td>21</td>
</tr>
<tr>
<td>7842</td>
<td>Multichannel Transceiver with Virtex-4 FPGAs - Half-length PCIe</td>
<td>21</td>
</tr>
<tr>
<td>5342</td>
<td>Multichannel Transceiver with Virtex-4 FPGAs - 3U VPX</td>
<td>21</td>
</tr>
<tr>
<td>7142-428</td>
<td>Multichannel Transceiver w. Four Multiband DDCs and Interpolation Filter - PMC/XMC</td>
<td>22</td>
</tr>
<tr>
<td>7242-428</td>
<td>Multichannel Transceiver w. Four Multiband DDCs and Interpolation Filter - 6U cPCI</td>
<td>22</td>
</tr>
<tr>
<td>7342-428</td>
<td>Multichannel Transceiver w. Four Multiband DDCs and Interpolation Filter - 3U cPCI</td>
<td>22</td>
</tr>
<tr>
<td>7642-428</td>
<td>Multichannel Transceiver w. Four Multiband DDCs and Interpolation Filter - PCI</td>
<td>22</td>
</tr>
<tr>
<td>7742-428</td>
<td>Multichannel Transceiver w. Four Multiband DDCs and Interpolation Filter - Full-length PCIe</td>
<td>22</td>
</tr>
<tr>
<td>7842-428</td>
<td>Multichannel Transceiver w. Four Multiband DDCs and Interpolation Filter - Half-length PCIe</td>
<td>22</td>
</tr>
<tr>
<td>5342-428</td>
<td>Multichannel Transceiver w. Four Multiband DDCs and Interpolation Filter - 3U VPX</td>
<td>22</td>
</tr>
</tbody>
</table>
## Putting FPGAs to Work in Software Radio Systems

### Links

More links on the next page ➤

### Model Description Page

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>7151</td>
<td>256-Channel DDC with Quad 200 MHz, 16-bit A/D - PMC</td>
<td>23</td>
</tr>
<tr>
<td>7251</td>
<td>256-Channel DDC with Quad 200 MHz, 16-bit A/D - 6U cPCI</td>
<td>23</td>
</tr>
<tr>
<td>7351</td>
<td>256-Channel DDC with Quad 200 MHz, 16-bit A/D - 3U cPCI</td>
<td>23</td>
</tr>
<tr>
<td>7651</td>
<td>256-Channel DDC with Quad 200 MHz, 16-bit A/D - PCI</td>
<td>23</td>
</tr>
<tr>
<td>7751</td>
<td>256-Channel DDC with Quad 200 MHz, 16-bit A/D - Full-length PCIe</td>
<td>23</td>
</tr>
<tr>
<td>7851</td>
<td>256-Channel DDC with Quad 200 MHz, 16-bit A/D - Half-length PCIe</td>
<td>23</td>
</tr>
<tr>
<td>5351</td>
<td>256-Channel DDC with Quad 200 MHz, 16-bit A/D - 3U VPX</td>
<td>23</td>
</tr>
<tr>
<td>7152</td>
<td>32-Channel DDC with Quad 200 MHz, 16-bit A/D - PMC</td>
<td>24</td>
</tr>
<tr>
<td>7252</td>
<td>32-Channel DDC with Quad 200 MHz, 16-bit A/D - 6U cPCI</td>
<td>24</td>
</tr>
<tr>
<td>7352</td>
<td>32-Channel DDC with Quad 200 MHz, 16-bit A/D - 3U cPCI</td>
<td>24</td>
</tr>
<tr>
<td>7652</td>
<td>32-Channel DDC with Quad 200 MHz, 16-bit A/D - PCI</td>
<td>24</td>
</tr>
<tr>
<td>7752</td>
<td>32-Channel DDC with Quad 200 MHz, 16-bit A/D - Full-length PCIe</td>
<td>24</td>
</tr>
<tr>
<td>7852</td>
<td>32-Channel DDC with Quad 200 MHz, 16-bit A/D - Half-length PCIe</td>
<td>24</td>
</tr>
<tr>
<td>5352</td>
<td>32-Channel DDC with Quad 200 MHz, 16-bit A/D - 3U VPX</td>
<td>24</td>
</tr>
<tr>
<td>7153</td>
<td>4-Channel DDC with Quad 200 MHz, 16-bit A/D - PMC/XMC</td>
<td>25</td>
</tr>
<tr>
<td>7253</td>
<td>4-Channel DDC with Quad 200 MHz, 16-bit A/D - 6U cPCI</td>
<td>25</td>
</tr>
<tr>
<td>7353</td>
<td>4-Channel DDC with Quad 200 MHz, 16-bit A/D - 3U cPCI</td>
<td>25</td>
</tr>
<tr>
<td>7653</td>
<td>4-Channel DDC with Quad 200 MHz, 16-bit A/D - PCI</td>
<td>25</td>
</tr>
<tr>
<td>7753</td>
<td>4-Channel DDC with Quad 200 MHz, 16-bit A/D - Full-length PCIe</td>
<td>25</td>
</tr>
<tr>
<td>7853</td>
<td>4-Channel DDC with Quad 200 MHz, 16-bit A/D - Half-length PCIe</td>
<td>25</td>
</tr>
<tr>
<td>5353</td>
<td>4-Channel DDC with Quad 200 MHz, 16-bit A/D - 3U VPX</td>
<td>25</td>
</tr>
<tr>
<td>7156</td>
<td>Dual SDR Transceiver, 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - PMC/XMC</td>
<td>26</td>
</tr>
<tr>
<td>7256</td>
<td>Dual SDR Transceiver, 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - 6U cPCI</td>
<td>26</td>
</tr>
<tr>
<td>7356</td>
<td>Dual SDR Transceiver, 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - 3U cPCI</td>
<td>26</td>
</tr>
<tr>
<td>7656</td>
<td>Dual SDR Transceiver, 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - PCI</td>
<td>26</td>
</tr>
<tr>
<td>7756</td>
<td>Dual SDR Transceiver, 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - Full-length PCIe</td>
<td>26</td>
</tr>
<tr>
<td>7856</td>
<td>Dual SDR Transceiver, 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - Half-length PCIe</td>
<td>26</td>
</tr>
<tr>
<td>5356</td>
<td>Dual SDR Transceiver, 400 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - 3U VPX</td>
<td>26</td>
</tr>
<tr>
<td>7158</td>
<td>Dual SDR Transceiver, 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - PMC/XMC</td>
<td>27</td>
</tr>
<tr>
<td>7258</td>
<td>Dual SDR Transceiver, 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - 6U cPCI</td>
<td>27</td>
</tr>
<tr>
<td>7358</td>
<td>Dual SDR Transceiver, 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - 3U cPCI</td>
<td>27</td>
</tr>
<tr>
<td>7658</td>
<td>Dual SDR Transceiver, 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - PCI</td>
<td>27</td>
</tr>
<tr>
<td>7758</td>
<td>Dual SDR Transceiver, 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - Full-length PCIe</td>
<td>27</td>
</tr>
<tr>
<td>7858</td>
<td>Dual SDR Transceiver, 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - Half-length PCIe</td>
<td>27</td>
</tr>
<tr>
<td>5358</td>
<td>Dual SDR Transceiver, 500 MHz A/D, 800 MHz D/A, Virtex-5 FPGAs - 3U VPX</td>
<td>27</td>
</tr>
<tr>
<td>71620</td>
<td>3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGAs - XMC</td>
<td>28</td>
</tr>
<tr>
<td>78620</td>
<td>3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGAs - PCIe</td>
<td>28</td>
</tr>
<tr>
<td>53620</td>
<td>3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGAs - 3U VPX</td>
<td>28</td>
</tr>
<tr>
<td>72620</td>
<td>3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGAs - 6U cPCI</td>
<td>28</td>
</tr>
<tr>
<td>73620</td>
<td>3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGAs - 3U cPCI</td>
<td>28</td>
</tr>
<tr>
<td>74620</td>
<td>6-Channel 200 MHz A/D, DUC, 4-Channel 800 MHz D/A, Two Virtex-6 FPGAs - 6U cPCI</td>
<td>28</td>
</tr>
</tbody>
</table>
# Putting FPGAs to Work in Software Radio Systems

## Links

More links on the next page

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>71621</td>
<td>3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Installed IP Cores - XMC</td>
<td>29</td>
</tr>
<tr>
<td>78621</td>
<td>3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Installed IP Cores - PCIe</td>
<td>29</td>
</tr>
<tr>
<td>53621</td>
<td>3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Installed IP Cores - 3U VPX</td>
<td>29</td>
</tr>
<tr>
<td>72621</td>
<td>3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Installed IP Cores - 6U cPCI</td>
<td>29</td>
</tr>
<tr>
<td>73621</td>
<td>3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Installed IP Cores - 3U cPCI</td>
<td>29</td>
</tr>
<tr>
<td>74621</td>
<td>4-Channel 200 MHz A/D, DUC, 4-Channel 800 MHz D/A, Installed IP Cores - 6U cPCI</td>
<td>39</td>
</tr>
<tr>
<td>78630</td>
<td>1 GHz A/D, 1 GHz D/A, Virtex-6 FPGA - PCIe</td>
<td>30</td>
</tr>
<tr>
<td>71630</td>
<td>1 GHz A/D, 1 GHz D/A, Virtex-6 FPGA - XMC</td>
<td>30</td>
</tr>
<tr>
<td>53630</td>
<td>1 GHz A/D, 1 GHz D/A, Virtex-6 FPGA - 3U VPX</td>
<td>30</td>
</tr>
<tr>
<td>72630</td>
<td>1 GHz A/D, 1 GHz D/A, Virtex-6 FPGA - 6U cPCI</td>
<td>30</td>
</tr>
<tr>
<td>73630</td>
<td>1 GHz A/D, 1 GHz D/A, Virtex-6 FPGA - 3U cPCI</td>
<td>30</td>
</tr>
<tr>
<td>74630</td>
<td>Two 1 GHz A/Ds, Two 1 GHz D/As, Two Virtex-6 FPGAs - 6U cPCI</td>
<td>30</td>
</tr>
<tr>
<td>72640</td>
<td>1-Channel 3.6 GHz and 2-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - 6U cPCI</td>
<td>31</td>
</tr>
<tr>
<td>73640</td>
<td>1-Channel 3.6 GHz and 2-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - 3U cPCI</td>
<td>31</td>
</tr>
<tr>
<td>74640</td>
<td>2-Channel 3.6 GHz and 4-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGAs - 6U cPCI</td>
<td>31</td>
</tr>
<tr>
<td>71640</td>
<td>1-Channel 3.6 GHz and 2-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - XMC</td>
<td>31</td>
</tr>
<tr>
<td>78640</td>
<td>1-Channel 3.6 GHz and 2-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - PCIe</td>
<td>31</td>
</tr>
<tr>
<td>53640</td>
<td>1-Channel 3.6 GHz and 2-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGA - 3U VPX</td>
<td>31</td>
</tr>
<tr>
<td>53650</td>
<td>2-Channel 500 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA - 3U VPX</td>
<td>32</td>
</tr>
<tr>
<td>71650</td>
<td>2-Channel 500 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA - XMC</td>
<td>32</td>
</tr>
<tr>
<td>78650</td>
<td>2-Channel 500 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA - PCIe</td>
<td>32</td>
</tr>
<tr>
<td>72650</td>
<td>2-Channel 500 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA - 6U cPCI</td>
<td>32</td>
</tr>
<tr>
<td>73650</td>
<td>2-Channel 500 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA - 3U cPCI</td>
<td>32</td>
</tr>
<tr>
<td>74650</td>
<td>4-Channel 500 MHz A/D, DUC, 4-Channel 800 MHz D/A, Two Virtex-6 FPGAs - 6U cPCI</td>
<td>32</td>
</tr>
<tr>
<td>72651</td>
<td>2-Channel 500 MHz A/D, with DDCs, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA - 6U cPCI</td>
<td>33</td>
</tr>
<tr>
<td>73651</td>
<td>2-Channel 500 MHz A/D, with DDCs, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA - 3U cPCI</td>
<td>33</td>
</tr>
<tr>
<td>74651</td>
<td>2-Channel 500 MHz A/D, with DDCs, DUCs, 2-Channel 800 MHz D/A, Virtex-6 FPGAs - 6U cPCI</td>
<td>33</td>
</tr>
<tr>
<td>71651</td>
<td>2-Channel 500 MHz A/D, with DDCs, DUCs, 2-Channel 800 MHz D/A, Virtex-6 FPGA - XMC</td>
<td>33</td>
</tr>
<tr>
<td>78651</td>
<td>2-Channel 500 MHz A/D, with DDCs, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA - PCIe</td>
<td>33</td>
</tr>
<tr>
<td>53651</td>
<td>2-Channel 500 MHz A/D, with DDCs, DUCs, 2-Channel 800 MHz D/A, Virtex-6 FPGA - 3U VPX</td>
<td>33</td>
</tr>
<tr>
<td>71660</td>
<td>4-Channel 200 MHz 16-bit A/D with Virtex-6 FPGA - XMC</td>
<td>34</td>
</tr>
<tr>
<td>78660</td>
<td>4-Channel 200 MHz 16-bit A/D with Virtex-6 FPGA - PCIe</td>
<td>34</td>
</tr>
<tr>
<td>53660</td>
<td>4-Channel 200 MHz 16-bit A/D with Virtex-6 FPGA - 3U VPX</td>
<td>34</td>
</tr>
<tr>
<td>72660</td>
<td>4-Channel 200 MHz 16-bit A/D with Virtex-6 FPGA - 6U cPCI</td>
<td>34</td>
</tr>
<tr>
<td>73660</td>
<td>4-Channel 200 MHz 16-bit A/D with Virtex-6 FPGAs - 3U cPCI</td>
<td>34</td>
</tr>
<tr>
<td>74660</td>
<td>8-Channel 200 MHz 16-bit A/D with Two Virtex-6 FPGAs - 6U cPCI</td>
<td>34</td>
</tr>
<tr>
<td>71661</td>
<td>4-Channel 200 MHz 16-bit A/D with Installed IP Cores - XMC</td>
<td>35</td>
</tr>
<tr>
<td>78661</td>
<td>4-Channel 200 MHz 16-bit A/D with Installed IP Cores - PCIe</td>
<td>35</td>
</tr>
<tr>
<td>53661</td>
<td>4-Channel 200 MHz 16-bit A/D with Installed IP Cores - 3U VPX</td>
<td>35</td>
</tr>
<tr>
<td>72661</td>
<td>4-Channel 200 MHz 16-bit A/D with Installed IP Cores - 6U cPCI</td>
<td>35</td>
</tr>
<tr>
<td>73661</td>
<td>4-Channel 200 MHz 16-bit A/D with Installed IP Cores - 3U cPCI</td>
<td>35</td>
</tr>
<tr>
<td>74661</td>
<td>8-Channel 200 MHz 16-bit A/D with Installed IP Cores - 6U cPCI</td>
<td>35</td>
</tr>
</tbody>
</table>
### Links

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>78662</td>
<td>4-Channel 200 MHz 16-bit A/D with Installed IP Cores - PCIe</td>
<td>36</td>
</tr>
<tr>
<td>71662</td>
<td>4-Channel 200 MHz 16-bit A/D with Installed IP Cores - XMC</td>
<td>36</td>
</tr>
<tr>
<td>53662</td>
<td>4-Channel 200 MHz 16-bit A/D with Installed IP Cores - 3U VPX</td>
<td>36</td>
</tr>
<tr>
<td>72662</td>
<td>4-Channel 200 MHz 16-bit A/D with Installed IP Cores - 6U cPCI</td>
<td>36</td>
</tr>
<tr>
<td>73662</td>
<td>4-Channel 200 MHz 16-bit A/D with Installed IP Cores - 3U cPCI</td>
<td>36</td>
</tr>
<tr>
<td>74662</td>
<td>8-Channel 200 MHz 16-bit A/D with Installed IP Cores - 6U cPCI</td>
<td>36</td>
</tr>
<tr>
<td>71670</td>
<td>4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - XMC</td>
<td>37</td>
</tr>
<tr>
<td>78670</td>
<td>4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - PCIe</td>
<td>37</td>
</tr>
<tr>
<td>53670</td>
<td>4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 3U VPX</td>
<td>37</td>
</tr>
<tr>
<td>72670</td>
<td>4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 6U cPCI</td>
<td>37</td>
</tr>
<tr>
<td>73670</td>
<td>4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA - 3U cPCI</td>
<td>37</td>
</tr>
<tr>
<td>74670</td>
<td>8-Channel 1.25 GHz D/A with DUCs, and Two Virtex-6 FPGAs - 6U cPCI</td>
<td>37</td>
</tr>
<tr>
<td>53690</td>
<td>L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - 3U VPX</td>
<td>38</td>
</tr>
<tr>
<td>71690</td>
<td>L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - XMC</td>
<td>38</td>
</tr>
<tr>
<td>78690</td>
<td>L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - PCIe</td>
<td>38</td>
</tr>
<tr>
<td>72690</td>
<td>L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - 6U cPCI</td>
<td>38</td>
</tr>
<tr>
<td>73690</td>
<td>L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA - 3U cPCI</td>
<td>38</td>
</tr>
<tr>
<td>74690</td>
<td>Dual L-Band RF Tuner with 4-Channel 200 MHz A/D and Two Virtex-6 FPGAs - 6U cPCI</td>
<td>38</td>
</tr>
<tr>
<td>71760</td>
<td>4-Channel 200 MHz 16-bit A/D with Virtex-7 FPGA - XMC</td>
<td>39</td>
</tr>
<tr>
<td>78760</td>
<td>4-Channel 200 MHz 16-bit A/D with Virtex-7 FPGA - PCIe</td>
<td>39</td>
</tr>
<tr>
<td>53760</td>
<td>4-Channel 200 MHz 16-bit A/D with Virtex-7 FPGA - 3U VPX</td>
<td>39</td>
</tr>
<tr>
<td>72760</td>
<td>4-Channel 200 MHz 16-bit A/D with Virtex-7 FPGA - 6U cPCI</td>
<td>39</td>
</tr>
<tr>
<td>73760</td>
<td>4-Channel 200 MHz 16-bit A/D with Virtex-7 FPGA - 3U cPCI</td>
<td>39</td>
</tr>
<tr>
<td>74760</td>
<td>8-Channel 200 MHz 16-bit A/D with Two Virtex-7 FPGAs - 6U cPCI</td>
<td>39</td>
</tr>
<tr>
<td>6821-422</td>
<td>215 MHz, 12-bit A/D with Wideband DDCs - VME/VXS</td>
<td>40</td>
</tr>
<tr>
<td>6822-422</td>
<td>Dual 215 MHz, 12-bit A/D with Wideband DDCs - VME/VXS</td>
<td>41</td>
</tr>
<tr>
<td>6826</td>
<td>Dual 2 GHz 10-bit A/D - VME/VXS</td>
<td>42</td>
</tr>
<tr>
<td>6890</td>
<td>2.2 GHz Clock, Sync and Gate Distribution Board - VME</td>
<td>43</td>
</tr>
<tr>
<td>6891</td>
<td>System Synchronizer and Distribution Board - VME</td>
<td>44</td>
</tr>
<tr>
<td>7190</td>
<td>Multifrequency Clock Synthesizer - PMC</td>
<td>45</td>
</tr>
<tr>
<td>7290</td>
<td>Multifrequency Clock Synthesizer - 6U cPCI</td>
<td>45</td>
</tr>
<tr>
<td>7390</td>
<td>Multifrequency Clock Synthesizer - 3U cPCI</td>
<td>45</td>
</tr>
<tr>
<td>7690</td>
<td>Multifrequency Clock Synthesizer - PCI</td>
<td>45</td>
</tr>
<tr>
<td>7790</td>
<td>Multifrequency Clock Synthesizer - Full-length PCIe</td>
<td>45</td>
</tr>
<tr>
<td>7890</td>
<td>Multifrequency Clock Synthesizer - Half-length PCIe</td>
<td>45</td>
</tr>
<tr>
<td>5390</td>
<td>Multifrequency Clock Synthesizer - 3U VPX</td>
<td>45</td>
</tr>
<tr>
<td>7191</td>
<td>Programmable Multifrequency Clock Synthesizer - PMC</td>
<td>46</td>
</tr>
<tr>
<td>7291</td>
<td>Programmable Multifrequency Clock Synthesizer - 6U cPCI</td>
<td>46</td>
</tr>
<tr>
<td>7391</td>
<td>Programmable Multifrequency Clock Synthesizer - 3U cPCI</td>
<td>46</td>
</tr>
<tr>
<td>7691</td>
<td>Programmable Multifrequency Clock Synthesizer - PCI</td>
<td>46</td>
</tr>
<tr>
<td>7791</td>
<td>Programmable Multifrequency Clock Synthesizer - Full-length PCIe</td>
<td>46</td>
</tr>
<tr>
<td>7891</td>
<td>Programmable Multifrequency Clock Synthesizer - Half-length PCIe</td>
<td>46</td>
</tr>
<tr>
<td>5391</td>
<td>Programmable Multifrequency Clock Synthesizer - 3U VPX</td>
<td>46</td>
</tr>
</tbody>
</table>
## Links

### Model Description Page

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>7192</td>
<td>High-Speed Synchronizer and Distribution Board - PMC/XMC</td>
<td>47</td>
</tr>
<tr>
<td>7892</td>
<td>High-Speed Synchronizer and Distribution Board - PCIe</td>
<td>47</td>
</tr>
<tr>
<td>5392</td>
<td>High-Speed Synchronizer and Distribution Board - 3U VPX</td>
<td>47</td>
</tr>
<tr>
<td>7292</td>
<td>High-Speed Synchronizer and Distribution Board - 6U cPCI</td>
<td>47</td>
</tr>
<tr>
<td>7392</td>
<td>High-Speed Synchronizer and Distribution Board - 6U cPCI</td>
<td>47</td>
</tr>
<tr>
<td>7492</td>
<td>High-Speed Synchronizer and Distribution Board - 6U cPCI</td>
<td>47</td>
</tr>
<tr>
<td>7893</td>
<td>System Synchronizer and Distribution Board - PCIe</td>
<td>48</td>
</tr>
<tr>
<td>9190</td>
<td>Clock and Sync Generator for I/O Modules - Rackmount</td>
<td>49</td>
</tr>
<tr>
<td>9192</td>
<td>High-Speed System Synchronizer Unit - Rackmount</td>
<td>50</td>
</tr>
<tr>
<td>RTS 2706</td>
<td>Eight-Channel RF/IF 200 MS/sec Rackmount Recorder</td>
<td>51</td>
</tr>
<tr>
<td>RTS 2709</td>
<td>Ultra Wideband One- or Two-Channel RF/IF, 3.2 GS/sec Rackmount Recorder</td>
<td>52</td>
</tr>
<tr>
<td>RTS 2715</td>
<td>Two-Channel 10 Gigabit Ethernet Rackmount Recorder</td>
<td>53</td>
</tr>
<tr>
<td>RTS 2716</td>
<td>Eight-Channel Serial FPDP Rackmount Recorder</td>
<td>54</td>
</tr>
<tr>
<td>RTR 2726</td>
<td>Four-Channel RF/IF 200 MS/sec Rugged Portable Recorder</td>
<td>55</td>
</tr>
<tr>
<td>RTR 2736</td>
<td>Eight-Channel Serial FPDP Rugged Portable Recorder</td>
<td>56</td>
</tr>
<tr>
<td>RTR 2746</td>
<td>Eight-Channel RF/IF 200 MS/sec Rugged Rackmount Recorder</td>
<td>57</td>
</tr>
<tr>
<td>RTR 2749</td>
<td>Ultra Wideband One- or Two-Channel RF/IF, 3.2 GS/sec Rugged Rackmount Recorder</td>
<td>58</td>
</tr>
<tr>
<td>RTR 2755</td>
<td>Two-Channel 10 Gigabit Ethernet Rugged Rackmount Recorder</td>
<td>59</td>
</tr>
<tr>
<td>RTR 2756</td>
<td>Eight-Channel Serial FPDP Rugged Rackmount Recorder</td>
<td>60</td>
</tr>
<tr>
<td>—</td>
<td>Pentek SystemFlow Recording Software</td>
<td>61</td>
</tr>
</tbody>
</table>

### Handbooks, Catalogs and Brochures

- Click here to [Software Defined Radio Handbook](#)
- Click here to [Critical Techniques for High-Speed A/D Converters in Real-Time Systems Handbook](#)
- Click here to [High-Speed Switched Serial Fabrics Improve System Design Handbook](#)
- Click here to [High-Speed, Real-Time Recording Systems Handbook](#)
- Click here to [Onyx Virtex-7 and Cobalt Virtex-6 Product Catalog](#)
- Click here to [Pentek Product Catalog](#)