

XILINX  
VIRTEX-7

XILINX  
ZYNQ

### APISSYS

Radar Emitter-Receiver  
Phased-Array Radar Receivers  
Conduction Cooled  
Wideband communication  
and Processing

### AV Series

Defense: Electronic Warfare systems, Wide band Radar  
Medical Imaging: Digital X-Ray image enhancement  
High Energy Physics

### OpenVPX

DRFM, 3 Gbps ADC + DAC, Virtex 7  
Quad 12-bit 2.5 Gbps ADC, EW-ESM  
Three QSFP, >240 Gbps optical fibers  
ZYNQ-7D45, SBC with FPGA, VPX 3U



PREVIEW

## AF209

Arbitrary Broadband Signal Generation  
L, S and C bands  
Automatic Test Equipment (ATE)

FMC HPC  
Single 12 bit 4.5 Gbps DAC  
Conduction or Air-Cooled



# ApisSys

# AF209

## Applications

- Test and Measurement
- Radar Transmitter
- Software Defined Radio

## Features

- 1 channel 12-bit, 4.5 Gbps DAC
- External clock and reference input
- Internal low jitter clock generation
- External trigger input and output
- VITA 57 FMC form factor
- Air cooled and Conduction cooled rugged versions
- FPGA firmware cores
- Windows® and Linux® drivers

## Overview

The AF209 is part of ApisSys' range of modular IOs solutions based on the VITA 57, FPGA Mezzanine Card standard.

The AF209 provides customers with a single channel 12-bit up to 4.5 Gbps DAC capability, ideally suited for test and measurement, Software Defined Radio or Radar Transmitter applications.

The AF209 DAC channel is AC coupled with an output bandwidth wider than 7 GHz for a full scale signal of -3 dBm (450 mVpp).

The AF209 provides an internal ultra low jitter clock generation and can be used with either an external clock or an external reference for higher flexibility.

The AF209 features an external trigger input and an external trigger output used to synchronize processing with external events.

The AF209 is fully supported on ApisSys 3U VPX FPGA processing engines, making it ideally suited for test and measurement, Software Defined Radio or Ultra Wideband Radar Transmitters applications.

## 12-bit 4.5 Gbps Digital-Analog Converter

The AF209 Digital to Analog conversion is performed by one e2v EV12DS400 12-bit 4.5 Gbps DAC.

The AF209 provides one front panel SSMC connector for the analog output.

The output signal is single ended AC coupled with an output bandwidth from 1 MHz to more than 7 GHz with -3 dBm output level.

## Clock

The AF209 provides an internal ultra low jitter clock generator locked on a 100 MHz internal reference.

The AF209 provides a front panel SSMC connector for an external reference from 10 to 100 MHz, a front panel SSMC connector for an external clock input from 500 MHz to 4.5 GHz and a front panel SSMC connector for an external clock output.

Estimated jitter from the internal clock generation (including 100 MHz reference and clock distribution) is below 200 fs for a 4.5 GHz clock. Added jitter on external clock is lower than 100 fs.

## Trigger and Synchronization

The AF209 provides a front panel SSMC connector for an external trigger input and one front panel SSMC connector for an external trigger output.

The trigger input and output signals are buffered with ultrafast PECL buffers.

## FMC interface

The AF209 features a VITA 57 – FMC (FPGA Mezzanine Card) compliant slot.

The FMC uses High Pin Count (HPC) interface with 1.8V or 2.5V Vadj.

The FMC MGT interfaces are unused.

## Firmware

The AF209 comes with a firmware package which includes VHDL cores allowing control and communication with all AF209 hardware resources.

A base design is provided which demonstrates the use of the AF209 and gives users a starting point for firmware development.

The AF209 firmware package is supported on the Xilinx VIVADO® 2015.2 design suite and later versions.

The AF209 firmware package has been fully validated on AV103 and other ApisSys FMC carrier products.

## Software

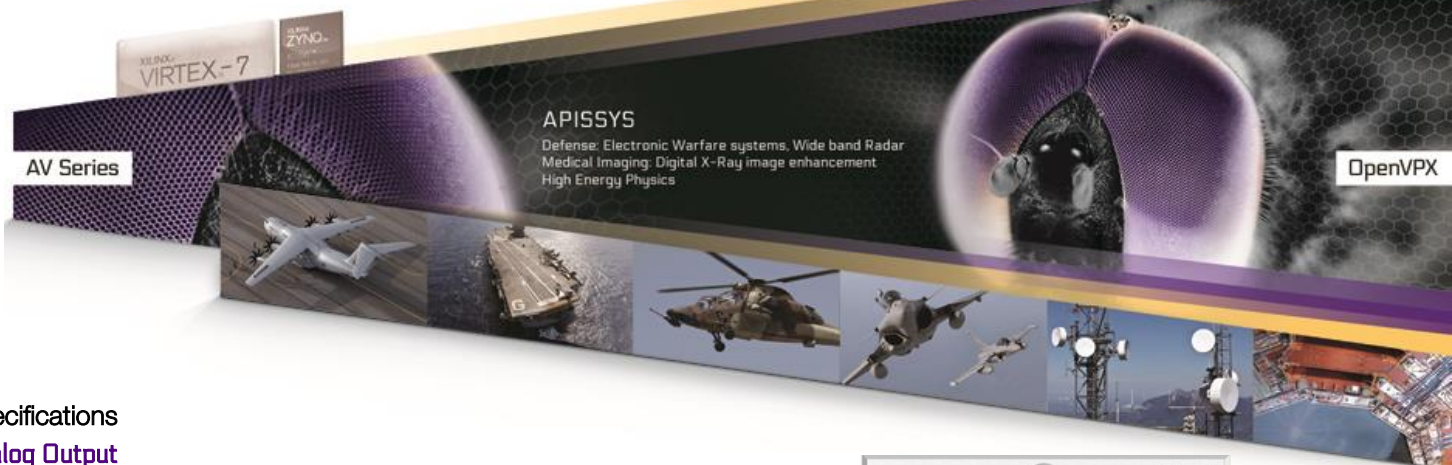
The AF209 is delivered with control software for Linux, compatible with AV108 and other ApisSys FMC carrier products.

An application example is provided as source code.

## Ruggedization

The AF209 is delivered in air cooled and conduction cooled standard or rugged versions for use in severe environmental conditions.

Standard VITA 47 supported ruggedization levels are EAC4, EAC6 and ECC3.



## Specifications

### Analog Output

- Output coupling: AC
- Full power bandwidth: > 6.5 GHz
- Full scale : -3 dBm
- Impedance: 50 Ohms
- Connector: SSMC

### Digital - Analog Conversion

- Single channel
- Resolution: 12 bit
- Sampling Frequency 500MHz to 4.5 GHz

### Sampling Performances

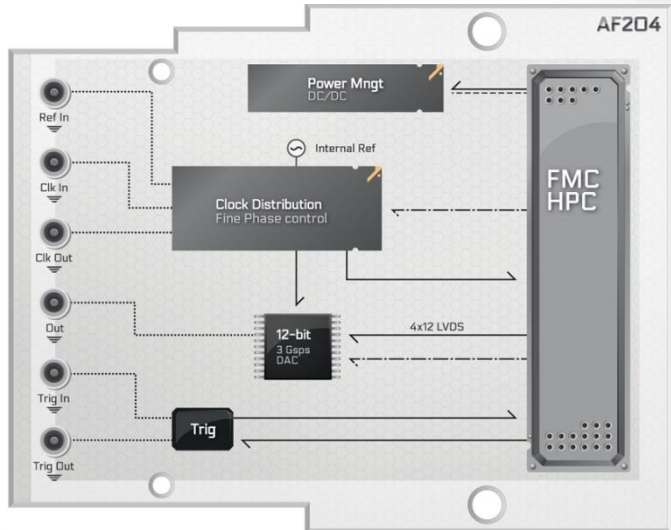
- 4.5 Gsps, Fout: 1500 MHz, -1dBFS:
  - NRZ mode SFDR: 55.5 dBc
  - NRTZ mode SFDR: 56 dBc
- 4.5 Gsps, Fout: 3.0 GHz, -1dBFS:
  - NRTZ mode SFDR: 56 dBc
  - RTZ mode SFDR: 52.5 dBc
  - RF mode SFDR: 50.5 dBc
- 4.5 Gsps, Fout: 5.0 GHz, -1dBFS:
  - RF mode SFDR: 50 dBc

### Clock

- Internal low jitter clock:
  - 500 MHz to 4.5 GHz
  - Internal jitter: < 200 fs
- External Input Clock:
  - frequency: 500 MHz to 4.5 GHz
  - Level: 10 dBm to 15 dBm
  - Added jitter (Ext clock) < 100 fs
  - Connector: SSMC, 50 Ohms
- External Output Clock:
  - frequency: sampling clock
  - Level: 0 dBm
  - Connector: SSMC, 50 Ohms
- External reference:
  - frequency: 10 MHz to 100 MHz
  - Level: 10 dBm to 15 dBm
  - Connector: SSMC, 50 Ohms

**APISSYS**  
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 High Energy Physics

OpenVPX



### Trigger

- External trigger Input
  - External Input: 0V to 2Vp
  - Connector: SSMC, 50 Ohms
- External Trigger Output
  - External Input: 0V to 2Vp
  - Connector: SSMC

### FMC interface

- HPC:
  - LA(0:33): LVDS 1.8V or 2.5V
  - HA(0:23): LVDS 1.8V or 2.5V
  - HB(0:21): LVCMOS 1.8V or 2.5V

### Software support

- Software Drivers:
  - Linux on AV108
- Application example:
  - Linux

### Firmware support

- VHDL cores for all hardware resources
- Base design
- Supported by Xilinx VIVADO 2015.2 and later

### Ruggedization

- As per VITA 47:
  - Air cooled : EAC4 and EAC6
  - Conduction cooled : ECC3

### Power dissipation

- +12V: 0.5 A max (6.1W)
- VADJ (1.8V or 2.5V): 0.2 A max (0.4W)
- +3.3V: 0.2 A max (0.7W)
- +3.3VAUX: 0.1 A max (0.4W)

### Weight

- Air cooled : 50g
- Conduction cooled : 55g

## Ordering information

Part Number		AF209	-	rr
Ruggedization level	Air Standard		-	AS
	Air Rugged		-	AR
	Conduction Standard		-	CS



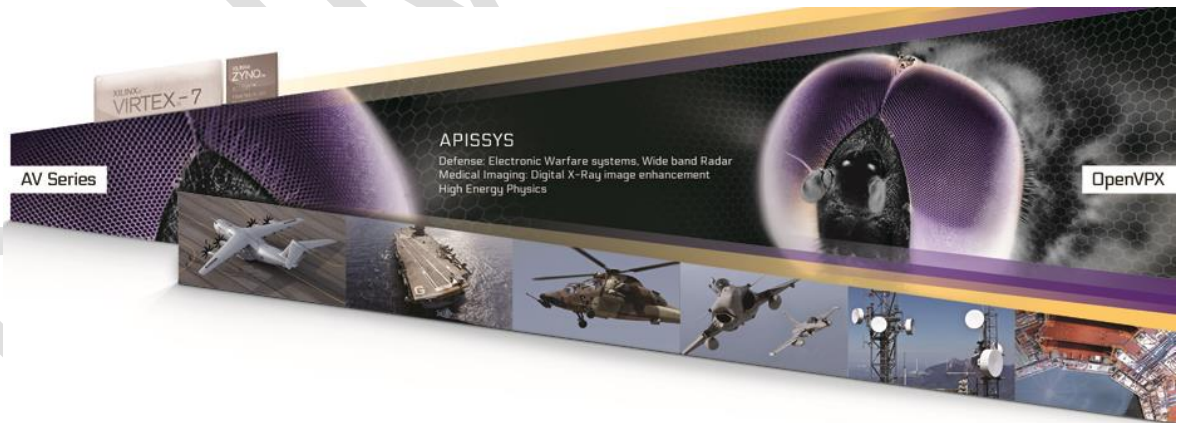
# High Speed Data Conversion

& Signal Processing Solutions

## Ruggedization levels

	Air flow, Standard AS (VITA 47 EAC4)	Air flow, Rugged AR (VITA 47 EAC6)	Conduction Standard CS (VITA 47 ECC3)	Conduction Rugged CR (VITA47 ECC4)
Operating Temperature	0°C to +55°C (8 CFM airflow at sea level)	-40°C to +70°C (8 CFM airflow at sea level)	-40°C to +70°C (Card Edge)	-40°C to +85°C (Card Edge)
Non Operating Temperature	-40°C to +85°C	-50°C to +100°C	-50°C to +100°C	-55°C to +105°C
Operating Vibration (Random)	5Hz - 100Hz +3 dB/octave 100Hz-1kHz = 0.04 g <sup>2</sup> /Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz-1kHz = 0.04 g <sup>2</sup> /Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz-1kHz = 0.1 g <sup>2</sup> /Hz 1kHz - 2kHz -6 dB/octave	5Hz - 100Hz +3 dB/octave 100Hz-1kHz = 0.1 g <sup>2</sup> /Hz 1kHz - 2kHz -6 dB/octave
Operating Shock	20g, 11 millisecond, half-sine	20g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine	40g, 11 millisecond, half-sine
Operating Relative Humidity	0% to 95% non-condensing	0% to 95% non-condensing	0% to 95% non-condensing	0% to 95% non-condensing
Operating Altitude	@ 0 to 10,000 ft with adequate airflow	@ 0 to 30,000 ft with adequate airflow	@ 0 to 60,000 ft	@ 0 to 60,000 ft
Conformal Coating	No	Optional (default acrylic AVR80)	Yes (default acrylic AVR80)	Yes (default acrylic AVR80)

[www.apissys.com](http://www.apissys.com)



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