Ensemble™

DATASHEET

MERCURY COMPUTER SYSTEMS

Ensemble 6000 Series OpenVPX SBC6120 Module

Balanced I/O and Processing in a Single VPX Slot

- VITA 46/48 (VPX-REDI) 6U serial RapidIO®-enabled module
- Dual-core MPC8640D or MPC8641D processor at up to 1.33 GHz
- Air-cooled and conduction-cooled models available
- Identical software infrastructure across Mercury products
- Architected to meet OpenVPX™ design principles

The Ensemble™ 6000 Series OpenVPX SBC6120 Single-Board Computer from Mercury Computer Systems is designed as a VITA 46 VPX-compliant module in a 6U form factor, also compatible with OpenVPX™ system architecture design principles. This module combines high-performance Power Architecture™ processing with balanced I/O from dual PMC/XMC sites and the scalable serial RapidIO® interconnect. Designed to meet the needs of a variety of applications and deployed environments, the SBC6120 module can function as a single-board computer or as part of an embedded processing cluster for high-end digital signal processing. With air-cooled and conduction-cooled variants available, the SBC6120 module can be deployed in a variety of environments with confidence.

The SBC6120 module is supported by the rich set of features available from the MultiCore Plus® software infrastructure, which allows ease of portability while offering an open software development architecture.

Power Architecture Processor

The Freescale™ MPC8640D or MPC8641D dual-core processor integrates two standard e600 processor cores, two DDR2 memory controllers, 1 MB of L2 cache, and a flexible system-on-chip I/O subsystem. The dual e600 cores that make up the heart of the chip are inherited from the MPC7448 processor, and each retains the high-performance AltiVec™ vector-processing unit. Algorithms optimized for the AltiVec engine port seamlessly to the MPC864xD. Additionally, increased bandwidth between both memory and external I/O and the processing cores allows efficient processing beyond that available with prior families of Freescale processors. The MPC8640D processor is a pin-compatible enhancement to the MPC8641D that delivers the same performance with a reduced power draw. The SBC6120 module can be configured with either 1 GB or 2 GB of DDR2 SDRAM per MPC864xD device.

System-Level Interconnect Architecture

The multi-plane architecture of the SBC6120 supports system-level reliability and separation of critical control signals from high-bandwidth, low-latency data transmissions.

Per the VITA 46.3 standard, four 4x lanes of serial RapidIO are available for high-bandwidth data movement among the processors and off-board. Supporting serial RapidIO data rates at up to 3.125 Gbaud, the on-board RapidIO crossbar links the SBC6120 module to other modules in the system, as well as, optionally, the XMC sites when configured for serial RapidIO. At the system level, serial RapidIO can be used as a data plane for high-bandwidth, low-latency data movement.

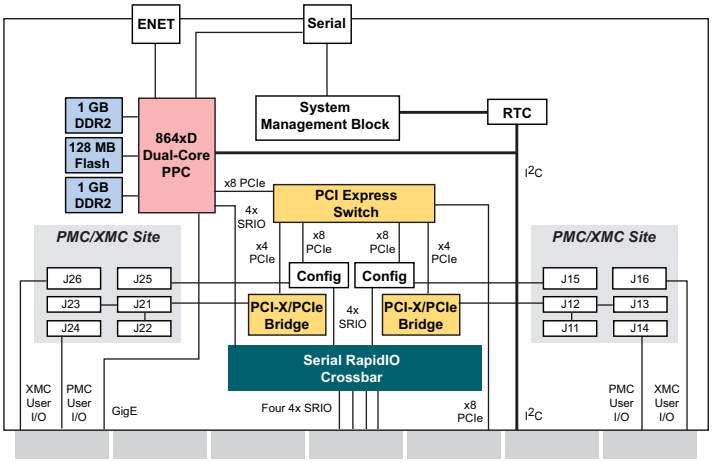

***Figure 1**. Ensemble 6000 Series OpenVPX SBC6120 Module functional block diagram*

A 1000BASE-BX Gigabit Ethernet link is provided to the backplane. At the system level, this Ethernet link can be used for point-to-point communication in a mesh, or switched via the Ensemble 6000 Series SFM6100 module to provide a separate control plane that can transmit and receive control and status information without impacting the application data flow on the data plane.

Mezzanine Card Flexibility

Each of the standard PMC/XMC sites on the SBC6120 module can be configured with off-the-shelf mezzanine cards using either PCI-X or PCI Express® protocols. PMC cards are supported with a PCI/PCI-X interface at up to 133 MHz on each site, with PMC user-defined I/O mapped to the backplane. XMCs are supported with x8, x4, x2, and x1 PCIe supported on the J5 connector per the VITA 42.3 standard. XMC user I/O is mapped to the backplane via the J6 connector. The XMC sites can also be factory-configured to support 1x or 4x serial RapidIO mezzanine cards per the VITA 42.2 standard.

Multiple I/O Options

In addition to the flexibility offered via the on-board mezzanine sites, the SBC6120 offers a variety of additional built-in I/O options:

- x8 PCI Express connection to the backplane is available for additional off-board communication.
- One Gigabit Ethernet connection to the front panel (a build option on air-cooled configurations only) or to the backplane.
- RS-232 serial port is routed to the front panel from the MPC864xD device. A build option exists to route this interface to the backplane, where it can support both RS-232 and RS-422/485 signaling.
- Eight GPIO lines act as discrete I/O, usable as input, output, or to generate interrupts on the module.
- Several additional bused signals enhance the functionality of the SBC6120 module.

System Management Plane

The SBC6120 module follows OpenVPX design principles in leveraging the robust, scalable, and well-tested system management infrastructure from the AdvancedTCA®/MicroTCA® architecture. Using the standard I²C bus and IPMI protocol, the on-board system-management block implements the Intelligent Platform Management Controller (IPMC), in accordance with the draft VITA 46.11 standard. This allows for the SBC6120 module to:

- Read sensor values
- Read and write sensor thresholds, allowing an application to react to thermal, voltage, or current variations that exceed those thresholds
- Reset the entire module
- Power up/down the entire module
- Retrieve module FRU (Field Replaceable Unit) information
- Be managed remotely by a Chassis Management Controller at the system level, such as implemented on the OpenVPX SFM6100 Module

VPX-REDI

The VPX (VITA 46) standard defines 6U and 3U board formats with a modern high-performance connector set capable of supporting today's high-speed fabric interfaces, such as RapidIO. VPX is most attractive when paired with the Ruggedized Enhanced Design Implementation standard – REDI (VITA 48). The SBC6120 module is implemented as a 6U conduction-cooled implementation of VPX-REDI, with air-cooled variants in the same VPX form factor available for less rugged environments. The SBC6120 module is unique in that it can be configured for 0.8" pitch VPX slots when air-cooled, which allows greater density at the system level, as well as for 1.0" pitch slots in both air-cooled and conduction-cooled configurations.

Targeted primarily for harsh-environment embedded applications, VPX-REDI offers extended mechanical configurations supporting higher functional density, such as two-level maintenance (2LM). 2LM allows relatively unskilled maintenance personnel to replace a failed module and restore the system to an operational state in a limited time period, minimizing potential damage to the module.

Additional Features

The SBC6120 module provides all the features typically found on a single-board computer. In addition to the sophisticated management subsystem and fabric interconnect, the SBC6120 module provides users with a toolkit enabling many different application use cases.

Features include:

- 128-MB of independent write-protectable boot/application flash, with protected boot vector to avoid accidental erasure
- Thermal and voltage sensors integrated on-board
- System Management Block for managing firmware updates, reading and writing sensor thresholds, reading sensor values, resetting the module, and powering the module up and down via remote system management
- Real-time clock with granularity to 1 ms and time measurement of up to 30 years
- General-purpose timers for synchronization
- Watchdog timer that can interrupt the MPC864xD upon expiration or reset the MPC864xD
- Open board architecture that supports network booting, as well as booting from the on-board flash memory

Open Software Environment

Mercury leverages over 25 years of multicomputer software expertise, including recent multicore processor expertise, across its many platforms. This strategy is fully applied to the SBC6120 module. Because the processor, memory, and surrounding technologies are leveraged across product lines, software developed on the SBC6120 module can interface seamlessly with other Mercury products. The same Linux® or VxWorks® development and run-time environment is implemented on the SBC6120 module as on other Mercury platforms, such as the Ensemble 6000 Series HCD6220 module and the Ensemble 5000 Series HCD5220 module.

The MultiCore Plus® (MCP) open software environment gives the SBC6120 module access to a wide ecosystem of stacks, middleware, libraries, and tools. The Scientific Algorithm Library (SAL) is optimized for the on-board Altivec engine and is available to give the SBC6120 module industry-leading signal processing performance. In addition, a key software package available for the SBC6120 module is MultiCore SAL (MCSAL). MCSAL offers the familiar SAL API interface, but is optimized for the multiple on-chip cores available with the MPC8640D.

MultiCore Plus®

Software support is available on the SBC6120 module for the following products:

- Open Development Suite for Linux is an Eclipse-based integrated development environment that includes a C/C++ optimizing compiler, a source-level debugger, a language-sensitive text editor, a performance profiler, a project builder, a version control system, a run-time error checker, and a graphical source browser. Mercury provides extensions that allow multiprocessor-aware process launch and debug, as well as a System Supervisor view that allows graphical remote management.
- Support is provided for Wind River Workbench integrated development environment when the module is running VxWorks
- Trace Analysis Tool and Library (TATL™) is a "logic analyzer for software" that provides insight into the dynamic interaction of up to a few hundred processors.
- Support for Mercury's standard numeric libraries, VSIPL and SAL (Scientific Algorithm Library), is optimized for the MPC8640D architecture of the SBC6120 module.
- Interprocessor Communication System (ICS) support is carried forward from the RACE++®/MCOE™ software environment. ICS provides a low-level interprocessor communication API that lets users take advantage of the high-bandwidth, low-latency serial RapidIO fabric with an easy-to-use software interface.
- Performance Porting Kit provides low-level handles for manipulation of the serial RapidIO fabric and can be used for simple data movement, or as a base on which to build a custom middleware layer.

The MCP software environment lets applications use industry-standard middleware such as MPI, DRI, CORBA, or standard TCP/IP sockets ported to run seamlessly over the fabric. MCP also offers a software tool that can help to migrate legacy applications created with MCOE into the MCP domain.

Open Standards Means Interoperability and Planning for the Future

The OpenVPX Industry Working Group is an industry initiative launched by defense prime contractors and COTS system developers, to take a proactive approach to solving the interoperability issues associated with the VITA 46 (VPX) family of specifications. This group is actively collaborating to create an overarching System Specification defining VPX system architecture through pinouts definition to establish a limited set of application-specific reference solutions. These OpenVPX™ standard solutions will provide clear design guidance to COTS suppliers and the user community, assuring interoperability across multi-vendor implementations. The OpenVPX™ System Specifications will be introduced into the VSO for ratification to replace the current VITA 46 base and dot specifications in the fall of CY2009.

Specifications

Module Specifications

Dual-core MPC8640D or MPC8641D processor
Two PMC/XMC sites
XMC factory-selectable for PCI Express or serial RapidIO connectivity
Air-cooled or conduction-cooled

Processor Node

Dual-core MPC864xD

MPC8641D	Up to 1.33 GHz
MPC8640D	Up to 1.06 GHz
Cores per device	2
DDR2 SDRAM	1 or 2 GB

PMC-X/XMC Sites

PMC-X sites	2
PCI-X-to-PCI-e bridge	Connects PMC sites to on-board PCI Express switch
PCI support	33 and 66 MHz
PCI-X support	66, 100, and 133 MHz

PMC user-defined I/O from P4 to backplane
PCIe XMC sites per VITA 42.3 or serial RapidIO XMC sites per VITA 42.2
With XMC user-defined I/O from J6 to backplane

Data/Control/Management Planes

Data plane
- Four 4x serial RapidIO links to backplane
- Switched via on-board crossbar

Control plane
- 1000BASE-BX Gigabit Ethernet connection to backplane

Management plane
- I^2C interface to backplane

I/O

10/100/1000BASE-TX Ethernet port routed to front panel (air-cooled only) or backplane
RS-232 serial interface to front panel interface
Optionally routed to the backplane with RS-232 and RS-422/485 support

Additional Resources

On-board 128-MB boot/application flash
Real-time clock
Watchdog timer
General-purpose 32-bit timers/counters
System Management Block
Thermal and voltage sensors

Environmental

Commercial and rugged air-cool and conduction-cooled variants available.

2306.00E-0809-DS-es6000vpx-sbc6120

MERCURY COMPUTER SYSTEMS

Corporate Headquarters
201 Riverneck Road
Chelmsford, MA 01824-2820 USA
+1 (978) 967-1401 • +1 (866) 627-6951
Fax +1 (978) 256-3599
www.mc.com

Europe
Mercury Computer Systems, Ltd.
Campbell Court, Unit 19 • Bramley, Tadley • HANTS RG26 5EG UNITED KINGDOM
+ 44 1 256 880090 • Fax + 44 1 25688 4004

Asia
Nihon Mercury Computer Systems K.K.
No. 2 Gotanda Fujikoshi Bldg. 4F • 5-23-1 Higashi Gotanda • Shinagawa-ku, Tokyo 141-0022 JAPAN
+81 3 3473 0140 • Fax +81 3 3473 0141

Challenges Drive Innovation™