Ensemble™

DATASHEET

MERCURY COMPUTER SYSTEMS™

Ensemble 6000 Series OpenVPX Intel Core 2 Duo SBC6521 Module

High-Density Processing, High Memory Bandwidth and I/O in Single VPX Slot

- 6U OpenVPX™-Compliant VITA 65/46/48 (VPX-REDI) module
- High-performance Intel® Core™2 Duo Penryn 1.80-GHz processor
- Air-cooled and conduction-cooled models available
- Integrated 48-lane PCIe switching infrastructure for on-board and off-board co-processing expansion-plane communications
- Mercury MultiCore Plus® software infrastructure support

The Ensemble™ 6000 Series OpenVPX™ Intel Core 2 Duo SBC6521 Module from Mercury Computer Systems combines the processing power of a single Intel® Core™2 Duo processor with the I/O capabilities of dual XMC/PMC sites in the standard 6U OpenVPX form factor. The SBC6521 is uniquely designed to support a variety of single-board computer (SBC) applications. The module is architected to meet the high-end data plane and expansion (co-processing) plane requirements that enable seamless application scaling with very low-latency, deterministic, high-bandwidth communications.

Intel® Core 2 Duo Processor

The SBC6521 features the Intel 64-bit, 1.80-GHz, SL9380 low-voltage Core 2 Duo Penryn CPU with the associated Intel 3100 chipset, which combines Memory Control Hub and I/O Control Hub (MCH/ICH) capabilities into a single device. This 45-nm processor architecture improves performance via higher energy efficiency and more responsive multitasking functionality. The reduction in footprint gained by utilizing the combined MCH/ICH chipset allows the SBC6521 to support a more comprehensive I/O infrastructure and more extensive SBC capabilities.

The SL9380 processor includes a very large 6-MB cache shared between the cores, allowing many high-performance calculations to remain cache resident. This accelerates processing by eliminating the latency required to access DRAM to fetch upcoming data. The SL9380 supports the SSE4.1 instruction set, supporting high-performance algorithm development that is portable to future Intel architectures. The module also provides 2 GB of DDR2 SDRAM with ECC support.

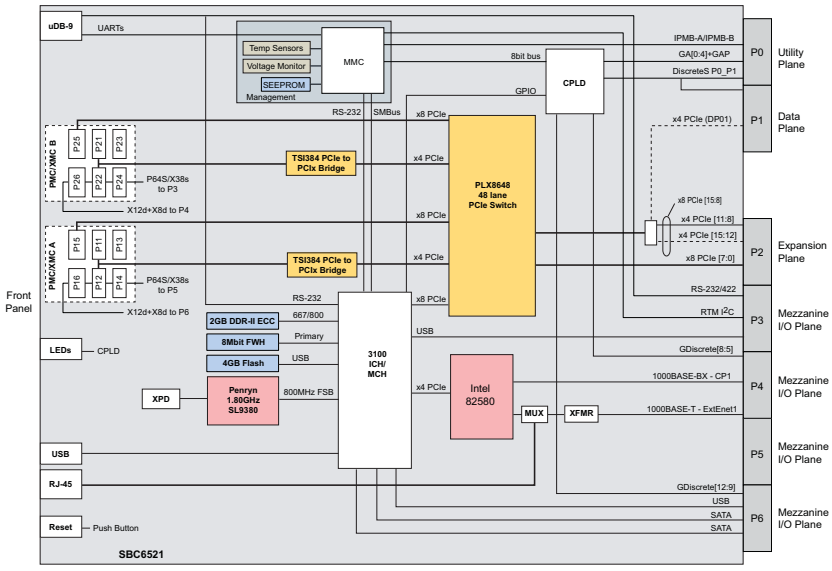

***Figure 1**. SBC6521 Module functional block diagram*

PCI Express Architecture

The SBC6521 has an integrated 48-lane PCIe switching infrastructure for both on-board switching and off-board expansion options. This Gen2 PCIe switch provides an x8 PCIe connection to each of the two XMC sites, as well as an x4 connection to each PMC site via a PCI-X to PCIe bridge. This allows mezzanines to operate at full bandwidth, optimizing the flow of I/O into the processing subsystem. Externally, the SBC6521 implements a full x16 PCIe connection to the OpenVPX expansion plane on the P2 VPX connector. This expansion plane interface enables the SBC6521's compatibility with Mercury's GPU or FPGA based co-processing modules. The x16 PCIe connection can be user-configured as dual x8 connections, and users can also configure non-transparent (NT) bridge functionality at run time. A build option is also available that further splits one of the x8 PCIe connections into dual x4 PCIe connections, routing one to the OpenVPX data-plane interface on the P1 connector. These configuration options let the module effectively act as an upstream/downstream PCIe switch to allow "chaining" of PCIe devices.

Mezzanine Card Flexibility

Each of the standard PMC/XMC sites on the SBC6521 module can be configured with off-the-shelf mezzanine cards using either PCI-X or PCI Express® (PCIe) protocols. PMC cards are supported with a PCI/PCI-X interface at up to 133 MHz on each site, with PMC user-defined I/O mapped to the backplane. XMCs are supported with x8, x4, and x1 PCIe (Gen1 or Gen2) supported on the J15/J25 connector per the VITA 42.3 standard. 20 differential pairs of XMC user I/O are mapped to the backplane from the J16/J26 connector.

Multiple I/O Options

In addition to the flexibility offered via the on-board mezzanine sites, the SBC6521 offers a variety of additional built-in I/O options:

- One 10/100/1000BASE-T Gigabit Ethernet connection can be routed to the front panel on air-cooled configurations or to the backplane on conduction-cooled configurations.
- One 1000BASE-BX SERDES Ethernet connection can be routed to the backplane per the OpenVPX control-plane specification.
- One RS-232 serial port can be routed to the front panel on air-cooled configurations, or to the backplane on conduction-cooled configurations. When routed to the backplane, the serial interface can be configured for either RS-232 or RS-422 signaling.
- One front-panel USB 2.0 interface is available on air-cooled configurations only.
- Two backplane USB 2.0 interfaces are available with both air-cooled and conduction-cooled configurations.
- Two SATA interfaces to the backplane are provided to easily interface with storage devices.
- Eight GPIO lines can act as discrete I/O, usable as input, output, or to generate interrupts on the module.
- Several additional bused signals enhance the functionality of the SBC6521 module.

System Management Plane

The SBC6521 module implements the advanced system management functionality architected in the OpenVPX Specification to enable remote monitoring, alarm management, and hardware revision and health status.

Using the standard I2C bus and IPMI protocol, the on-board system-management block implements the Intelligent Platform Management Controller (IPMC), in accordance with the VITA 46.11 standard. This allows the SBC6521 module to:

- Read sensor values
- Read and write sensor thresholds, allowing an application to react to thermal, voltage, or current variations that exceed those thresholds
- Reset the entire module
- Power up/down the entire module
- Retrieve module field replaceable unit (FRU) information
- Be managed remotely by a Chassis Management Controller at the system level, such as implemented on the OpenVPX SFM6100 module

VPX-REDI

The VPX (VITA 46) standard defines 6U and 3U board formats with a modern high-performance connector set capable of supporting today's high-speed fabric interfaces, such as RapidIO® fabric. VPX is most attractive when paired with the Ruggedized Enhanced Design Implementation standard – REDI (VITA 48). The SBC6521 module is implemented as a 6U conduction-cooled implementation of VPX-REDI, with air-cooled variants in the same VPX form factor available for less rugged environments.

Targeted primarily for harsh-environment embedded applications, VPX-REDI offers extended mechanical configurations supporting higher functional density, such as two-level maintenance (2LM). 2LM allows relatively unskilled maintenance personnel to replace a failed module and restore the system to an operational state in a limited time period, minimizing potential damage to the module.

Additional Features

The SBC6521 module provides all the features typically found on a single-board computer. In addition to the sophisticated management subsystem and fabric interconnect, the SBC6521 module provides users with a toolkit enabling many different application use cases.

Features include:

- Thermal and voltage sensors integrated on-board
- Real-time clock with granularity to 1 ms and time measurement of up to 30 years
- General-purpose counters/timers for synchronization
- Watchdog timer to support processor interrupt or reset
- VPX REF_CLK and AUX_CLK signals, supporting system-wide synchronization between modules
- Multiple boot paths, include netboot, USB boot, and boot from SATA or the on-board 4-GB flash device

Open Software Environment

Mercury leverages over 25 years of multicomputer software expertise, including recent multicore processor expertise, across its many platforms. This strategy is fully applied to the SBC6521 module. Because the integral software libraries and technologies are leveraged across product lines, software developed on the SBC6521 module can interface seamlessly with other Mercury products. The same Linux® or VxWorks® development and run-time environment is implemented on the SBC6521 module as on other Mercury platforms across the Ensemble 3000, 5000, and 6000 Series.

MultiCore Plus®

The MultiCore Plus® (MCP) open software environment gives the SBC6521 module access to a wide ecosystem of stacks, middleware, libraries, and tools. A key software package available for the SBC6521 module is MultiCore SAL (MCSAL). MCSAL offers the familiar SAL API interface, but is optimized for the multiple on-chip cores available with the Intel Core 2 Duo processor.

Software support is available on the SBC6521 module for the following products:

- Open Development Suite for Linux is an Eclipse-based integrated development environment that includes a C/C++ optimizing compiler, a source-level debugger, a language-sensitive text editor, a performance profiler, a project builder, a version control system, a run-time error checker, and a graphical source browser. Mercury provides extensions that allow multiprocessor-aware process launch and debug, as well as a System Supervisor view that allows graphical remote management.
- Support is provided for Wind River Workbench integrated development environment when the module is running VxWorks.
- Trace Analysis Tool and Library (TATL™) is a "logic analyzer for software" that provides insight into the dynamic interaction of up to a few hundred processors.
- Support for Mercury's standard numeric libraries, VSIPL and SAL (Scientific Algorithm Library), as well as their multi-core variants, is optimized for the Intel Core 2 Duo architecture of the SBC6521 module.
- The MCP software environment lets applications use industry-standard middleware such as MPI, DRI, CORBA, or standard TCP/IP sockets ported to run seamlessly over the fabric. MCP also offers a software tool that can help to migrate legacy applications created with MCOE™ into the MCP domain.

Open Standards Mean Interoperability and Planning for the Future

The OpenVPX Industry Working Group is an industry initiative launched by defense prime contractors and COTS system developers, to take a proactive approach to solving the interoperability issues associated with the VITA 46 (VPX) family of specifications. This group has created an overarching System Specification defining VPX system architecture through pinout definitions to establish a limited set of application-specific reference solutions. These OpenVPX standard solutions provide clear design guidance to COTS suppliers and the user community, assuring interoperability across multi-vendor implementations. The OpenVPX System Specification was ratified by the VSO in February 2010.

Specifications

Intel Core 2 Duo Processor

Dual-core	1.80 GHz
Intel computing technology	64-bit
Front side bus	800 MHz
DDR2-400	2 GB w/ ECC, 200 MHz
BIOS LPC flash	8 Mb
NAND flash	4 GB

Ethernet Connections

1000BASE-BX Ethernet to P4 connector OpenVPX control plane	1
10/100/1000BASE-T Ethernet connection to front panel (air-cooled module) or backplane (conduction-cooled module)	1

Ethernet functions supported by the chipset include:
UDP, TCP, SCTP, ARP, IPv4, IPv6, IEEE1588, flow control, 802.1P (priority), and 802.1Q (VLAN)

System Management

On-board IPMI Controller
Voltage and temperature sensors and monitoring
Geographical address monitor
Power/reset control
FRU and on-board EEPROM interfaces

OpenVPX Multi-Plane Architecture

System Management via IPMB-A and IPMB-B link on P0 management plane
Dual 1000BASE-BX Ethernet to P4 control plane
x4 PCIe to P1 data plane (optional)
Dual x8 PCIe to 2 expansion plane

PMC-X/XMC Sites

PMC-X sites	2

PCI-X-to-PCIe bridge
Connects PMC sites to on-board PCI Express switch

PMC PCI support	33 and 66 MHz
PMC PCI-X support	66, 100, and 133 MHz

PMC user-defined I/O from P4 to backplane
PCIe XMC sites per VITA 42.3 with XMC user-defined I/O from J6 to backplane

Additional I/O Capabilities

RS-232 serial interface to front panel (air-cooled) or backplane (conduction-cooled)	1

Configurable for RS-422 signaling when routed to backplane

Front-panel USB 2.0 interface (air-cooled configurations only)	1
USB 2.0 interfaces to backplane	2
SATA interfaces to backplane	2
Single-ended GPIO interfaces to backplane	8

System signals to backplane
NVMRO, ChassisTest, Environmental Bypass, MemoryClear

Mechanical

6U VPX (air-cooled and conduction-cooled)
1.0" slot pitch
OpenVPX and VPX-REDI

Power Consumption (estimate)*

12V payload	80 (maximum)
XMC budget	30W per XMC site

*Power consumption values are estimates of worst-case condition with 15% power efficiency as part of the calculation.

Environmental

Air-Cooled – Commercial

Temperature

Operating	0°C to 40°C*
Storage	-40°C to +85°C

*Customer must maintain required cfm level.

Humidity

Operating	10-95%, non-condensing
Vibration	0.003 g2/Hz; 20-2000 Hz, 1 hr/axis
Shock	20g, z-axis; 32g, x-, y-axes; 11 ms half-sine pulse

Altitude

Operating	0-10,000 ft*

*Customer must maintain required cfm level.

Conduction-Cooled – Mercury Rugged Level

Temperature

Operating	-40°C to +71°C at card edge*
Storage	-55°C to +125°C

*Customer chassis must maintain card edge at 71°C.

Humidity

Operating	0-100%
Vibration	0.1g2/Hz, based on 5-2000 Hz, 1 hr/axis
Shock	50g, z-axis; 80g, x-, y-axes; 11 ms half-sine
Altitude	0-70,000 ft

Compliance

OpenVPX System Specification encompasses VITA 46.0, 46.3, 46.4, 46.6, 46.11
Compatible with VITA 65
VITA 46/48.1/48.2 (REDI)
VITA 42/42.3

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