ADQ108

Datasheet

ADQ108 is a single channel high speed digitizer in the ADQ V6 Digitizer family. The ADQ108 has an outstanding combination of dynamic range and unique bandwidth, which enables demanding measurements such as RF/IF sampling of very wide band signals.

Features

- 6.4 GSPS sampling rate
- 8 bits resolution
- 2 GHz analog bandwidth
- Internal and external clock reference
- Clock reference output
- External trigger input and output
- Multi record >1 MHz PRF
- Time stamp
- 1 GSamples data memory
- Data interface USB 2.0 / cPCIe / PXIe
- FPGA available for customized applications
- Support for C/C++ and MATLAB

Applications

- RADAR
- LIDAR
- Wireless communication
- Optical transmission
- High-speed data recording
- Test and measurement
- Ultrasonic ranging

Software support

- MATLAB
- C/C++

Ordering information

ORDERING INFORMATION	
ADQ108 USB	ADQ108
AVAILABLE OPTIONS	
cPCIe / PXIe	–PXIE
Decimation IP	–DEC
8 GSPS	–8G
RELATED PRODUCTS	
ADQ Development Kit	ADQ108 Dev Kit

Example: ADQ108–PXIE

Introduction

The ADQ108 digitizer features single channel, 8 bits, 6.4 GSPS, 2 GHz analog input bandwidth, and 1 GSamples buffer memory. The ADQ108 is optimized for dynamic performance over a wide bandwidth, which makes it ideal for broadband applications such as IF/RF sampling and high-speed data recording. The ADQ108 offers an easy-to-use API that allows easy integration into any application. The digitizer connects to the host via a high-speed USB 2.0 interface or an eight-lane cPCIe / PXIe interface. The ADQ108 is equipped with an advanced Xilinx V6 LX240T FPGA which is partly available for customized real time applications.

ADQ Development Kit

SP Devices' ADQ Development Kit is an optional software tool that rapidly enhance the customization process of your next DSP application for the onboard FPGA. More details about this product can be found in the product brief for the ADQ Development Kit.

Contact
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Teknikringen 6, SE-583 33 Linköping, SWEDEN
www.spdevices.com

1 Technical data[1]

KEY PARAMETERS	
Number of channels	1
Digitizer Resolution	8
Sampling rate	6.4 / 6 GSPS
Clock reference	Internal / External / PXIe
Data memory	1 GSamples
Pre-trigger buffer	Up to batch size
Trigger hold off	2^{34} samples
Multi record batch size	1 to entire memory
Multi record max PRF	1.8 MHz
Trigger	Software / External / Level
Number of GPIOs	5
Front panel connectors	SMA/Micro-D Plug9w/MMCX

ANALOG INPUT[1]			
ENOB	245 MHz	7.2	bits
	748 MHz	7.0	bits
	1.5GHz	6.8	bits
	3 GHz	6.2	bits
SFDR	245 MHz	60	dB
	748 MHz	58	dB
	1.5GHz	56	dB
	3 GHz	51	dB
SNR	245 MHz	46	dB
	748 MHz	45	dB
	1.5GHz	44	dB
	3 GHz	41	dB
THD	245 MHz	–58	dBc
	748 MHz	–57	dBc
	1.5GHz	–52	dBc
	3 GHz	–50	dBc
Impedance AC		50	Ω
Bandwidth (–3 dB)		2	GHz
Input voltage range		700	mV_{pp}

1. Constant input power, **Figure 2**

EXTERNAL REFERENCE		
Frequency typ (max TBD)	10	MHz
Signal level (min – max)	0.8 – 3.3	V_{PP}
Impedance AC	50	Ω
Internal clock jitter	TBD	fs RMS

EXTERNAL TRIGGER INPUT		
Input impedance DC	50	Ω
Input range (min – max)	–2.5 – +3.3	V
Threshold rising edge	0.5	V
Time resolution	2	Samples

TRIGGER OUTPUT		
Output impedance	20	Ω
Output (low – high)	0.1 – 3.2	V

GPIO		
Output impedance	30	Ω
Output (low – high)	0.1 – 3.2	V
Input impedance	10	kΩ
Input (low – high)	1 – 2.3	V

HI-SPEED USB 2.0 INTERFACE		
Sustained data rate	25	MByte/s
Connector	Type B	

POWER SUPPLY		
Supply voltage	12	V
Power consumption	30	W

ENVIRONMENTAL / MECHANICAL		
Operating temperature	0 – 45	°C
Storage temperature	–20 – 70	°C
Relative humidity, non-condensing	5% – 95%	
Board size	100 x 163	mm^2
Case size	103 x 166 x 53	mm^3

OPERATING SYSTEM	
Windows XP	SP 2 and higher
Windows Vista	All versions

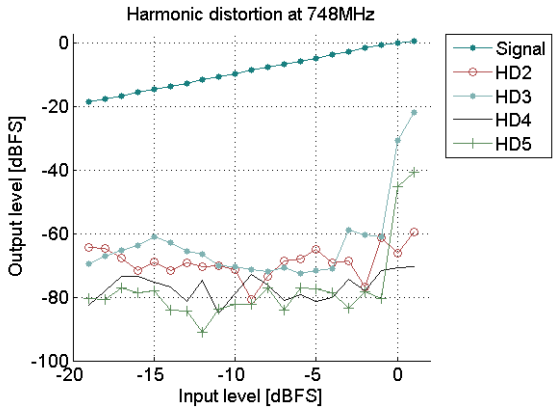
APPLICATION SOFTWARE	
ADCaptureLab	Data capture and analysis
MATLAB	Data capture interface
C/C++	Data capture interface

CERTIFICATION AND COMPLIANCE
CE

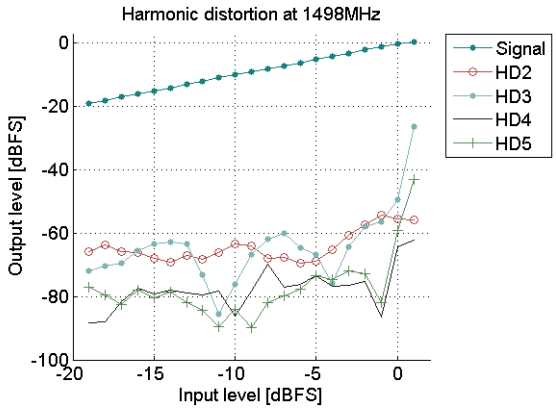
1. All values are typical unless otherwise noted.

2 Dynamic performance

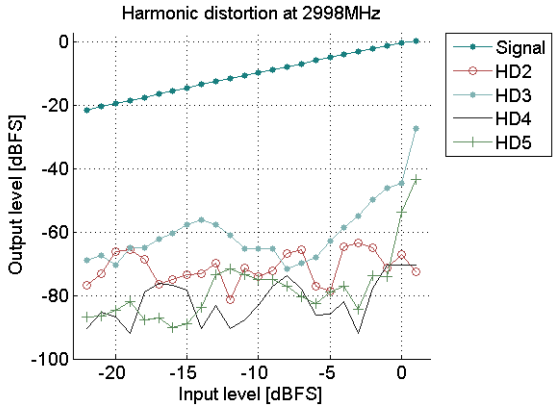
2.1 Linearity



(a) Input signal frequency 748 MHz



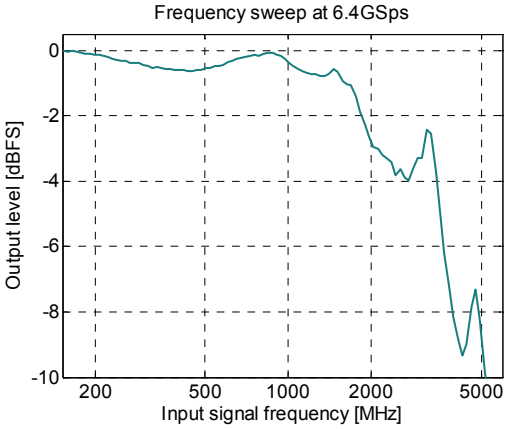
(c) Input signal frequency 1498 MHz



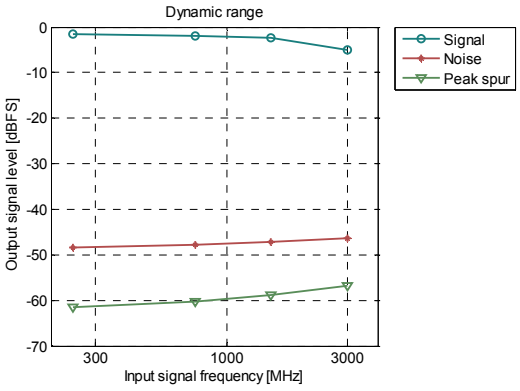
(c) Input signal frequency 2998 MHz

Figure 1: Harmonic distortion at different frequencies. Sampling rate 6.4 GSPS.

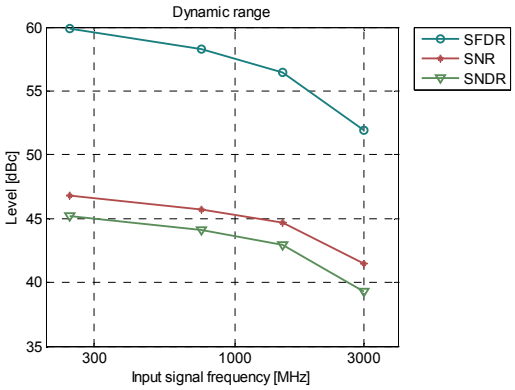
2.2 Frequency response



(a) Signal transfer function



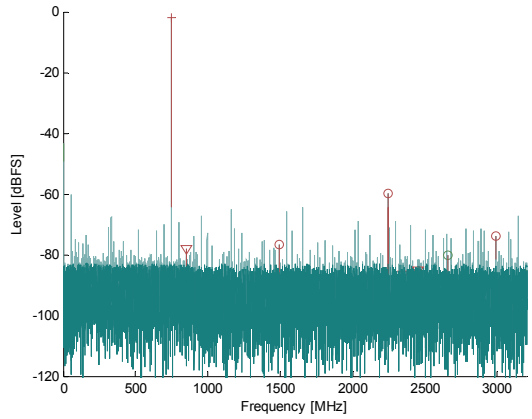
(b) SNR and SFDR at constant input power.



(c) Dynamic range

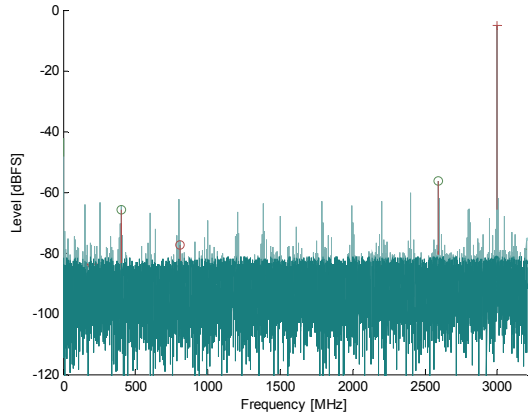
Figure 2: Input signal frequency sweep. Sampling rate 6.4 GSPS.

2.3 Output Spectrum



Signal frequency	748 MHz
Sampling rate	6.4 GSPS
HD2	–74 dBc
HD3	–58 dBc
THD	–57 dBc
SNR	45.7 dB
ENOB	7.0 bits

Figure 3: Typical spectrum at 748 MHz



Signal frequency	2998 MHz
Sampling rate	6.4 GSPS
HD2	–60 dBc
HD3	–51 dBc
THD	–50 dBc
SNR	39 dB
ENOB	6.2 bits

Figure 4: Typical spectrum at 2998 MHz

3 Absolute Maximum ratings

Exposure to conditions exceeding these rating may reduce life time or permanently damage the device.

ABSOLUTE MAXIMUM RATINGS		
	Min	Max
Supply voltage (to GND)	–0.4 V	14 V
Analog input (sine wave < 2GHz)		750 mV_{RMS}
Analog input (sine wave >2GHz)		1.5 V_{RMS}
Trigger input (to GND)	–3 V	3.7 V
Clock input (AC)		3.3 V_{PP}
Ambient temperature (operation)	0 °C	45 °C

The ADQ108 has a built in fan to cool the device. If the air flow is blocked or the fan malfunctions, the temperature surveillance unit will protect the ADQ108 from overheating by shutting down parts of the device.

The SMA connectors have an expected life time of 500 operations. For frequent connecting and disconnecting of cables, connector savers are recommended.

4 Architecture

4.1 Overview

The ADQ108 consists of a analog front end board and a ADQ DSP board. ADCs and clock are placed on the daughter card and the digital back end is on the ADQ DSP board.

4.2 Analog Front End, AFE

The analog input is single-ended AC coupled 50 Ohm. The single-ended signal is converted to a differential signal in a balun.

4.3 ADC

The ADC configuration is four 8 bit ADCs which are time interleaved to reach 6.4 GSPS effective sampling rate. The time interleaving is enabled by SP Devices' time interleaving algorithm ADX4.

4.4 Clock

The clock generator consists of a crystal oscillator as a clock reference and a PLL with built in VCO. The PLL has also built in dividers for generating necessary clock frequencies on the board. The sampling frequency is set by configuring these frequency dividers.

There is also an external SMA connector for an external clock. The external clock frequency shall be sampling frequency/4.

4.5 FPGA

The data outputs of the ADCs are connected to a Xilinx XC6VLX240T-1 which runs the time interleaving algorithm ADX4 and handles the communication with the host and the batch data RAM. This FPGA is partly open for user applications through the ADQ Development Kit.

4.6 Memory

There is 1 GSamples data batch memory. The data batch length for each recording is set to any value within this range. For more information about memory handling, see **Section 4.8**.

4.7 Interface

The ADQ108 is connected to the host computer through a Hi-Speed USB interface which is used for control and uploading of data.

The USB connection can be configured in a streaming mode. The sustained data rate is then 25 MBytes/s[1]. This is typically used together with a data reduction algorithm, implemented through the ADQ Development Kit.

See **Section 6.1** for Compact PCI Express (cPCIe) / PXI Express (PXIe) interface.

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(a) Front panel

(b) Rear panel

Figure 5: ADQ108 stand alone box

4.8 Trigger

4.8.1 Overview

The ADQ108 has several trigger options

- Software trigger
- Level trigger
- External trigger

When armed, the system is waiting for the selected trigger event. At the trigger event, a data batch of selected length is recorded in the batch memory. A pre-trigger buffer is available. The length of the pre-trigger buffer is fully controllable[2]. The pre-trigger buffer is a part of the total batch length.

The trigger hold-off is up to 2^{34} samples and is set in steps of 16 samples.

4.8.2 Software trigger

Data capture is triggered by a software command. This is suitable for measurements on continuous waves.

1. This is highly dependent of other tasks performed by the operating system on the host computer.

2. There is a fixed amount of delay between the trigger and data depending on the length of the wires and the internal signal paths. This delay will change for a custom application using the ADQ Development Kit.

4.8.3 Level trigger

Data capture is triggered by an event on the input data. This is useful for capturing pulses. The level trigger combined with the pre-trigger or trigger hold-off setting can capture any pulse shape.

4.8.4 External trigger

Data capture is triggered by positive edge on the trigger input connector. This is intended for synchronizing the signal source with the ADQ108. It can also be used for synchronizing several digitizers.

4.8.5 Multi record

The ADQ108 can be set up in a multi record mode. At each trigger, a record of data is captured in the memory. The length of each record and number of records is user defined. Multi record works together with pre-trigger buffer and trigger hold off.

The pulse repeat frequency (PRF) can be set up to 1.8 MHz depending on the record length.

4.9 Time stamp

A 64 bits time counter enables time stamp for each event. At each trigger event, the counter value is read and stored together with the data record.

The time counter starts at power up and may directly be used for relative time measurement. The counter can be reset by software. The counter can also be synchronized to an external start pulse. The external start pulse can operate in two modes; single start signal or repeated restart of the time counter. In the repeated restart mode, the counter is divided into a 42 bits time counter and a 22 bits start pulse counter.

The start pulse is connected to GPIO pin #2.

4.10 GPIO

The ADQ108 is equipped with five bi-directional GPIOs. The GPIOs are controlled from software, but can also be accessed from the ADQ Development Kit.

The connector is Micro D plug 9 way. A suitable socket with lead is for example MOLEX 83421-9044.

The trigger input and output connectors can also be used as general purpose input and output respectively.

#	Function
1	GPIO
2	GPIO
3	GPIO
4	GPIO
5	GPIO
6	GND
7	GND
8	GND
9	GND

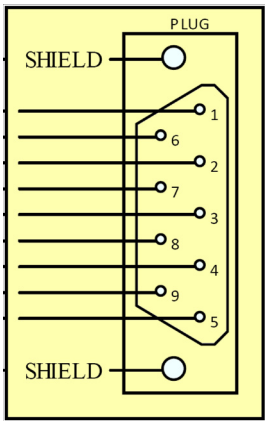

Figure 6: GPIO connector diagram.

5 Software tools

5.1 ADCaptureLab

The ADQ108 is supplied with the ADCaptureLab software that provides quick and easy control of the digitizer. The tool also offers both time domain and frequency domain analysis, see **Figure 7**. Data can be saved in different file formats for off-line analysis. Comparison of results is easily done by importing data from file and analyze it in ADCaptureLab.

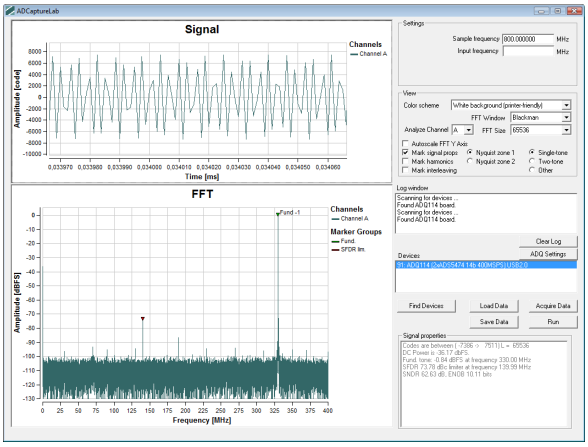

Figure 7: ADCaptureLab. Typical board.

5.2 Software development kit (SDK)

The ADQ108 data acquisition system is easily integrated into your own application by using the included software development kit. The SDK includes programming examples and reference projects for C/C++ and MATLAB.

6 Options

6.1 cPCIe / PXIe interface

The ADQ108 is available with cPCIe / PXIe interface.

cPCIe / PXIe INTERFACE		
Bus width	8	lanes
Bus peak capacity	16	Gbit/s
Sustained data rate, 4 lanes	400	MByte/s
PXIe card size	1 slot 3U 4TE	

Figure 8: cPCIe / PXIe interface

Order code: –PXIE

6.2 Decimation IP

A Decimation IP is available for integration in the FPGA. The Decimation IP can decimate up to 2^{34} times. The Decimation IP together with the Low frequency option is ideal for low frequency noise measurements.

The Decimation IP implements a close to ideal low pass filter, which suppresses the wide band quantization noise in digitizer. The theory of decimation gives that each factor of 4 in decimation yields one extra bit in resolution. The result is an increased dynamic range.

The Decimation IP makes the ADQ108 very flexible and a large set of measurements specifications can be met with the same device.

DECIMATION IP CONFIGURATIONS (EXAMPLES)		
Decimation order	Sampling rate	Resolution
$2^0 = 1$	6 GSPS	8 bits
$2^4 = 16$	375 MSps	10 bits
$2^{12} = 4096$	1.46 MSps	14 bits

Availablity to be confirmed.

Order code: –DEC

6.3 Memory up-grade

See ADQ DSP datasheet for options.

6.4 FPGA options

See ADQ DSP datasheet for options.

6.5 High sampling rate 8 GSPS

The ADQ108 can be upgraded to 8 GSPS. Availability to be confirmed.

Order code: –8G